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# P90X0 MVME224-1 / MVME224-2
# 4M / 8M byte Memory Modules

## Field Support Manual


PHILIPS

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# 4M / 8M byte Memory Modules

## Field Support Manual

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Great care has been taken to ensure that the information contained in this handbook is accurate and complete. Should any errors or omissions be discovered or should any user wish to make a suggestion for improving this handbook, he is invited to send the relevant details to:

**PHILIPS TELECOMMUNICATIE EN DATA SYSTEMEN**
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## Preface

This manual provides general information, hardware preparation, installation instructions, functional description, and support information for the MVME224 series of DRAM memory modules.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system or in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *Related Documentation* paragraph in Chapter 1 of this manual.

The information in this document about the MVME224 module jumper setting is not explicit for the P90X0 configuration.

To be sure having the correct jumper setting, refer to the Customer Engineer Manual P90X0 or to the Installation Instructions delivered with the MVME224 board.

The part numbers in the section 4.3 are the Motorola part numbers. These numbers can be incorrect.
For the correct numbers see the Spare Parts P90X0 manual distributed by Customer Service Logistics.
A copy of the current MVME224-2 part of this manual is included at the rear of this manual. There is no list available for the MVME224-1 because this board is not released within the P90X0 family.

**WARNING**

**THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL INVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERRFERENCE.**



First Edition

# SAFETY SUMMARY
# SAFETY DEPENDS ON YOU

***The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.***

**GROUND THE INSTRUMENT.**

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

**DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.**

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

**KEEP AWAY FROM LIVE CIRCUITS.**

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

**DO NOT SERVICE OR ADJUST ALONE.**

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

**USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.**

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

**DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.**

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

**DANGEROUS PROCEDURE WARNINGS.**

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

**WARNING**

**Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.**

## TABLE OF CONTENTS

## LIST OF ILLUSTRATIONS

## LIST OF TABLES

# CHAPTER 1 - GENERAL INFORMATION

## 1.1 INTRODUCTION

This user's manual provides general information, preparation and installation instructions, functional description, and support information for the MVME224-1 (4 Megabyte) and MVME224-2 (8 Megabyte) DRAM Memory Modules with VME/VSB Interface. These modules are referred to as the MVME224 throughout the remainder of this manual.

## 1.2 FEATURES

The features of the MVME224 include:

- Memory Capacity - 4Mb or 8Mb using 1-megabit DRAMs in ZIP packages.
- Dual ported VMEbus interface with 16-/24-/32-bit address selection and 16-/32-bit data.
- Multiplexed VSB interface with 32-bit address/data.
- Longword (32-bit), Word (16-bit), and byte (8-bit) data transfers.
- Memory base address switch-selectable on any 1Mb boundary throughout the VMEbus and VSB address space.
- Error Protection -- Parity is provided on a byte basis.
- Command and Status Register -- Control over parity and error status reporting.
- Fast Read -- Selectable to start reads on PAS* on VSB for fast access or DS* to allow a cache detection.
- Fast Write -- Both VMEbus and VSB provide early DTACK on a write access.

## 1.3 SPECIFICATIONS

General specifications for the MVME224 are provided in Table 1-1.

**TABLE 1-1. MVME224 SPECIFICATIONS**

| Characteristic | Specification |
|---|---|
| Storage capacity: | |
| MVME224-1 | 4 Megabytes |
| MVME224-2 | 8 Megabytes |
| Data transfer size | 8-, 16-, and 32-bit |

**TABLE 1-1. MVME224 SPECIFICATIONS (cont.)**

| Characteristic | Specification |
|---|---|
| Error detection | Odd byte parity |
| Data Input/Output | 16-32-bit VMEbus, 32-bit VSB |
| Input address | 16-/24-/32-bit VMEbus, 32-bit VSB |
| Power requirements: | |
| MVME224-1 | +4.75 to 5.25 Vdc at 5 A maximum (3.9A typical) |
| MVME224-2 | +4.75 to 5.25 Vdc at 5 A maximum (3.9A typical) |
| Relative humidity | 5% to 95% (non-condensing) |
| Temperature: | |
| Operating | Ø degree to 5Ø degrees C inlet air temperature with forced air cooling. |
| Storage | -4Ø degrees to 85 degrees C |
| Physical size (PCB): | |
| Height x width | 6.3Ø inches (16.ØØ cm) x 9.19 inches (23.34 cm) |
| Thickness | Ø.Ø62 inch (Ø.157 cm) |
| Part projections: | |
| Component side | Ø.5Ø inch (1.27 cm) maximum |
| Solder side | Ø.Ø67 inch (Ø.17 cm) maximum |

## 1.4 GENERAL DESCRIPTION

The MVME224 module is a high performance dynamic memory module, dual ported to both the VMEbus and VSB bus. Both modules can be mapped to start on any 1Mb boundary and extend by the module (board) size. The MVME224 uses an advanced arbitration method which buries the arbitration time for the next cycle in the current cycle, thus increasing throughput.

## 1.5 REFERENCE DOCUMENTATION

The following publications provide additional helpful information. If not shipped with this product, they may be purchased from the Motorola Literature Distribution Center, 616 West 24th Street, Tempe Arizona 85282; telephone (6Ø2) 994-6561.

| DOCUMENT TITLE | MOTOROLA PUBLICATION NUMBER |
|---|---|
| VMEbus Specification (Rev C.1) | HB212/D |
| VME Subsystem Bus (VSB) Specification | MVMESB |

## 1.6 MANUAL TERMINOLOGY

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

| | | |
|---|---|---|
| $ | dollar | specifies a hexadecimal number |
| % | percent | specifies a binary number |
| & | ampersand | specifies a decimal number |

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

# CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION

## 2.1 INTRODUCTION

This chapter provides the unpacking, hardware preparation, and installation instructions for the MVME224 memory modules. It also describes the start-up procedures.

## 2.2 UNPACKING INSTRUCTIONS

**NOTE**

If shipping carton is damaged upon receipt, request that the carrier's agent be present during unpacking/inspection of equipment.

Carefully unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the shipping carton and packing materials for storing or reshipping of the equipment.

**CAUTION**

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

Inspect for any shipping damage. If no damage exists, then the module can be prepared for operation according to the following sections of this chapter.

## 2.3 HARDWARE PREPARATION

This section describes the hardware preparation of the MVME224 memory module prior to installation. Observance of this description will ensure the user that all components are properly configured for operation.

Jumper blocks are used to select the various functions and options of the MVME224 memory module. Before the MVME224 is installed, the user should verify the jumper block configurations and alter the jumpers, as required, for the user's particular system operation.

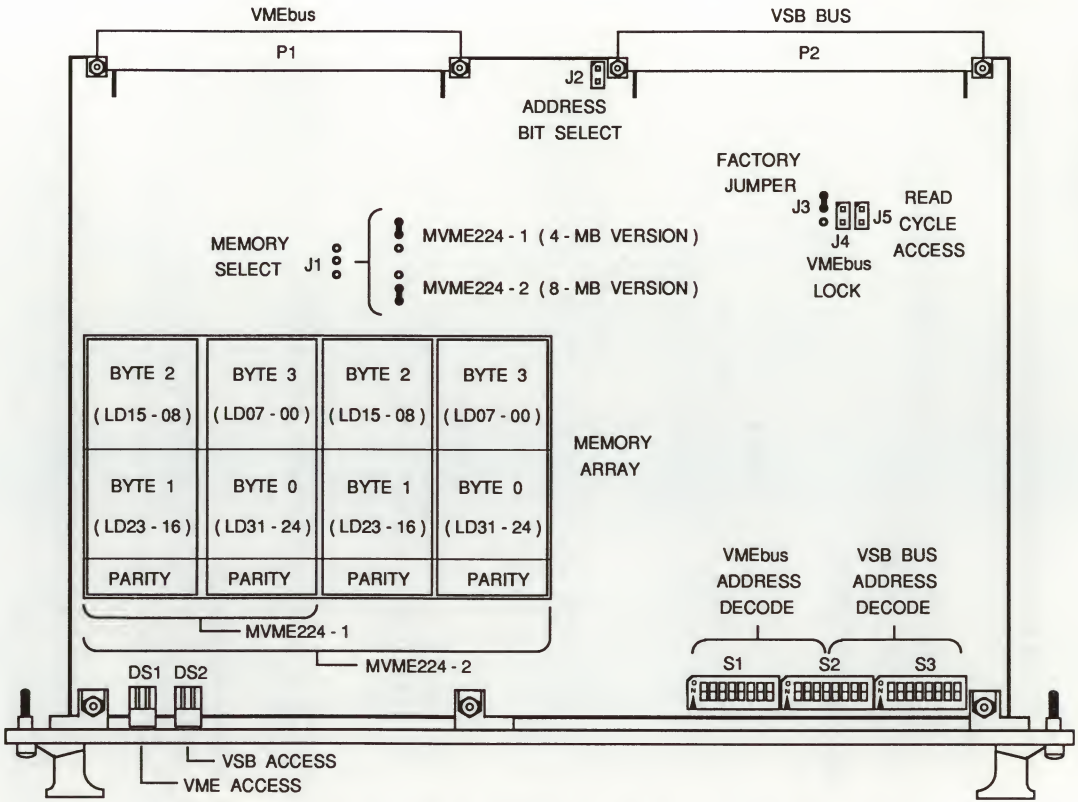



FIGURE 2-1. MVME224 JUMPER, CONNECTOR, AND SWITCH LOCATION DIAGRAM

The MVME224 has been factory tested and is shipped with factory-installed jumper configurations that are illustrated in Figure 2-1. The MVME224 is operational with these factory-installed jumpers. Table 2-1 lists the jumper blocks by designation, function, and factory configuration. A more detailed description of these jumper blocks is provided in the following sections.

Also, three DIP-type switches (S1, S2, and S3) are located on the MVME224. For detailed information regarding the use of these three switches, refer to section 2.3.7.

### 2.3.1 Jumper Block Settings

The following table lists and describes the MVME224 jumper blocks.

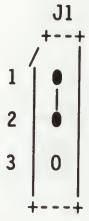
**TABLE 2-1. MVME224 FACTORY JUMPER PLACEMENTS**

| Jumper | Function | Factory Configuration |
|---|---|---|
| J1 | Memory Selection<br>(Soldered Staple Jumper) | J1(1-2) (MVME224-1, 4Mb version)<br>J1(2-3) (MVME224-2, 8Mb version) |
| J2 | Address Bit Selection | No Jumper(s) Installed. |
| J3 | Factory Jumper<br>(Soldered Staple Jumper) | J3(1-2) (All versions) |
| J4 | VMEbus Lock | No Jumper(s) Installed. |
| J5 | Read Cycle Access | No Jumper(s) Installed. |

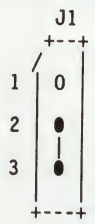
### 2.3.2 Memory Selection (J1)

Jumper block J1 determines the memory selection of the MVME224 memory module. A staple pin is factory soldered across jumper J1 pins 1-2 on the MVME224-1 (4Mb version) and across jumper J1 pins 2-3 on the MVME224-2 (8Mb version).

Jumper Block J1
Memory Selection
4-Megabyte Version
(Factory Setting)



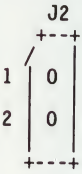

Jumper Block J1
Memory Selection
8-Megabyte Version
(Factory Setting)




### 2.3.3 Address Bit Selection (J2)

Jumper block J2 determines the address bit selection. With no jumper installed, 24- or 32-bit addressing is allowed. With a jumper installed across jumper J2 pins 1-2, 24-bit address modifiers will not be decoded and the module will not respond to 24-bit addresses.

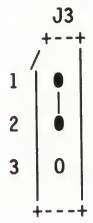
Jumper Block J2
Address Bit Selection
No Jumper Installed
(Factory Setting)



### 2.3.4 Factory Jumper (J3)

Jumper block J3 is for factory use only. A staple pin is factory soldered across J3 pins 1 and 2 in all versions of the MVME224 Revision B memory modules. This jumper block does not exist on MVME224 Revision C memory modules.

Jumper Block J3
Factory Jumper Only
(Factory Setting)




### 2.3.5 VMEbus Lock (J4)

In systems that support the VMELOCK signal option (such as the MVME130, MVME131, MVME135, or MVME141), installing a jumper pin across J4 pins 1 and 2 will allow control of locking the VMEbus. Normally, the VSB bus is locked out until Address Strobe (AS*) on the VMEbus returns to high, as there is no way to detect a read-modify-write cycle. If this jumper is installed, only those cycles that allow VMELOCK* to go high are locked and the MVME224 is allowed to start a VSB bus cycle sooner; not waiting for the VMEbus AS* to return high. The VMELOCK signal is driven by the bus master on the reserved bus pin P2-B3.

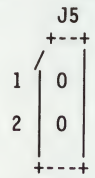
Jumper Block J4
VMEbus Lock
No Jumper Installed
(Factory Setting)

### 2.3.6 Read Cycle Access (J5)

Jumper block J5 serves two functions. First, it determines whether a read cycle will start from PAS* or DS* on the VSB bus. In some systems doing caching, the master will drive addresses and PAS* during the time it is decoding a potential local cache hit. If a cache hit is found, it simply removes the strobes without driving DS* or completing the cycle. Installing a mini-jumper across pins 1 and 2, starts read cycles on DS* to avoid starting false cycles. Systems not employing these address-only cache cycles should start reads on PAS* (i.e., with the jumper not installed).

Secondly, jumper block J5 also determines whether the WAIT* signal will be driven. In a system with one or more slaves who decode and drive ASACKØ* or ASACK1* in less than 5Ø nanoseconds, jumper J5 should be installed. Installing jumper J5 causes the MVME224 to drive the WAIT* signal and forces the master to hold addresses stable until decoding is done by the MVME224. This slows system performance slightly, so it should be avoided unless necessary. In a system where all slaves are MVME224s, or no slaves are capable of decoding addresses and driving ASACKØ* or ASACK1* in less than 5Ø nanoseconds from PAS*, do not install jumper J5.

Jumper Block J5
Read Cycle Access
No Jumper Installed
(Factory Setting)



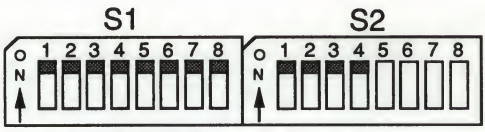
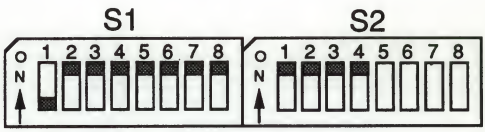
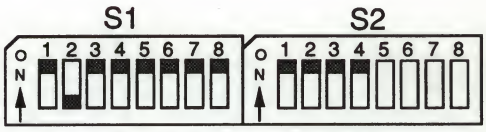
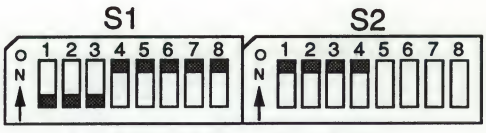

### 2.3.7 VME/VSB Address Decode Switches

DIP switches S1, S2, and S3 are used in selecting the starting address for the VMEbus and the VSB bus mapping. Addressing is independently selectable on 1Mb boundaries.

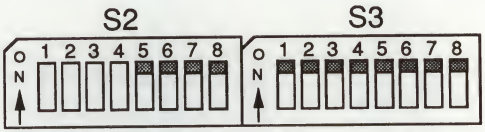
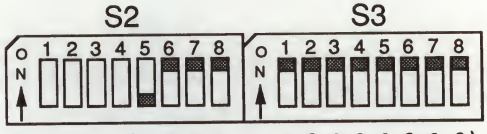
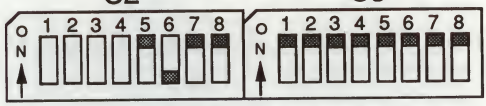
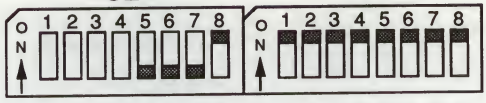
The VME portion of the switches is also used in selecting the starting address for the CSR mapping. The CSR is mapped dependent on the mapping of the addressing to the RAMs on the VMEbus. The following examples illustrate how the switch positions can be set for any required address.

**Example:** VMEbus Address Mapping (S1-1 to S1-8 and S2-1 to S2-4) on 1Mb boundaries.

CSR Mapping - Base address is BEØ1, increasing 4 bytes for each 2Mb increase of RAM base address.

| BEGINNING ADDRESS | SWITCH S1 | SWITCH S2 |
|---|---|---|
| 0 0 0 0 0 0 0 0 = (CSR ADDR: BE01) |  | |
| | (0 0 0 0 0 0 0 0 | 0 0 0 0) |
| 0 0 1 0 0 0 0 0 = (CSR ADDR: BE01) |  | |
| | (1 0 0 0 0 0 0 0 | 0 0 0 0) |
| 0 0 2 0 0 0 0 0 = (CSR ADDR: BE05) |  | |
| | (0 1 0 0 0 0 0 0 | 0 0 0 0) |
| 0 0 7 0 0 0 0 0 = (CSR ADDR: BE0C) |  | |
| | (1 1 1 0 0 0 0 0 | 0 0 0 0) |

**Example:** VSB Bus Address Mapping (S2-5 to S2-8 and S3-1 to S3-8) on 1Mb boundaries.

| BEGINNING ADDRESS | SWITCH S2 | SWITCH S3 |
|---|---|---|
| 0 0 0 0 0 0 0 0 = |  | |
| | (0 0 0 0 | 0 0 0 0 0 0 0 0) |
| 0 0 1 0 0 0 0 0 = |  | |
| | (1 0 0 0 | 0 0 0 0 0 0 0 0) |
| 0 0 2 0 0 0 0 0 = |  | |
| | (0 1 0 0 | 0 0 0 0 0 0 0 0) |
| 0 0 7 0 0 0 0 0 = |  | |
| | (1 1 1 0 | 0 0 0 0 0 0 0 0) |

## 2.4 INSTALLATION INSTRUCTIONS

After the MVME224 has been properly configured for operation, it is ready for installation in a VMEmodule chassis.

1. Ensure that power is turned **OFF** to the chassis and that the board ejector handles are in their non-eject positions.

> **CAUTION**
>
> INSERTING OR REMOVING THE BOARD WHILE POWER IS APPLIED CAN DAMAGE THE BOARD CIRCUITRY. AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

2. The Bus Grant and IACK backplane jumpers may either be installed or removed in the card slot in which the MVME224 is installed. The MVME224 does not use these signals.

3. Slide the board into the board slides of the selected slot until the P1/P2 connectors align and seat into their backplane sockets. Press firmly on the top and bottom sections of the front panel until the connectors seat fully into their backplane sockets. Avoid pressing against the board ejector handles as they may slide into their board eject positions. When installing, check the position of the two captive screws at the top and bottom ends of the front panel. They may jam against the chassis frame and prevent the board from seating fully.

4. Once installed, screw in the two captive screws to secure the board in place. Avoid over-tightening the screws as they may strip out the screw sockets. The screws also serve to electrically connect the front panel to the frame of the chassis by pressing the conductive top and bottom sections of the front panel against the conductive frame of the chassis. This integrates the front panel into the EMI (Electromagnetic Interference) shield of the chassis. This also reduces the susceptibility of the board to static discharge that can result from touching the front panel. These EMI protections rely on the use of a chassis that is properly designed to control the susceptibility and emission of EMI.

5. Connect the power cable to the AC power source and turn the unit **ON**.

# CHAPTER 3 - FUNCTIONAL DESCRIPTION



## 3.1 INTRODUCTION

This chapter provides an overall block diagram view of the MVME224 memory module. The discussion includes sections with detailed descriptions of the 4/8Mb DRAM array, the DRAM timing and control circuitry with dual port and refresh arbitration, the VMEbus interface and address decode, the VSB bus interface and address decode, parity generation and checking, and the Control/Status Register. For the purpose of the following description, the MVME224 is regarded as consisting of functional blocks as illustrated in Figure 3-1. For further details, refer to the schematic diagram in Chapter 4 and to the VMEbus Specification Manual (Motorola publication HB212/D).

## 3.2 DRAM ARRAY

The MVME224-1 (4Mb version) provides a DRAM array of 36 1-megabit DRAMs in zip packages. The MVME224-2 (8Mb version) provides a DRAM array of 72 1-megabit DRAMs in zip packages. The DRAM array is arranged in 4 bytes with 1 parity bit per byte on the 4Mb version, or 8 bytes with 1 parity bit per byte on the 8Mb version.

CAS before RAS refresh is utilized, using the address counter internal to the DRAMs, therefore, no refresh addresses must be supplied.

## 3.3 DRAM TIMING, CONTROL, AND ARBITRATION

DRAM timing, arbitration of the internal bus between VMEbus and VSB bus, and refresh arbitration are all accomplished from two timing chains. The TØ* timing handles arbitration while the RASTØ* timing handles RAM signals. One of the potential users of the arbitration scheme (VMEbus, VSB bus, and refresh) will have control at any time. When a request for a cycle is generated from either of the address decode circuits or the refresh circuit, the TØ* timing chain is started. This timing chain will cause arbitration to take place. If the user that generated the request is the same as the one which has the internal control, then the RASTØ* timing is also started. This will cause a memory cycle, or CSR cycle to take place. The third possibility is that a cycle can be started on the TØ* timing chain by a user not having control causing an arbitration cycle to start. If within 5Ø nanoseconds, a cycle is decoded on the circuit which does have control, the RASTØ* timing chain will start causing what started as an arbitration only cycle to become also a valid memory cycle.

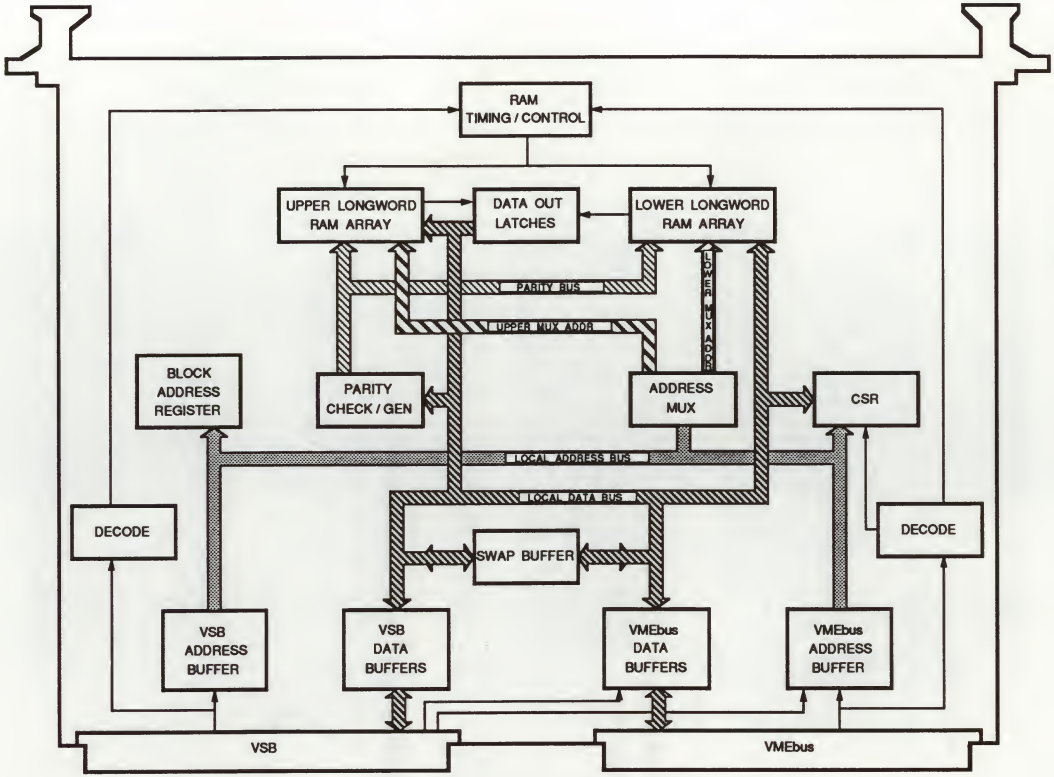



FIGURE 3-1. MVME224 BLOCK DIAGRAM

In each case, an arbitration is done midways in the cycle to determine who will have control for the next cycle. In the case of a refresh cycle, it is always arbitrated back to either VME or VSB. It will go to VSB if a VSB cycle is pending, to VME if a VME cycle is pending with no VSB pending, or, if neither has a cycle pending, back to the one that preceded it. The result of this arbitration method is greater performance and, under heavy loading of both busses, performance actually increases over light loading of both busses.

The read cycle timing diagram is illustrated in Figure 3-2. The write cycle timing diagram is illustrated in Figure 3-3.

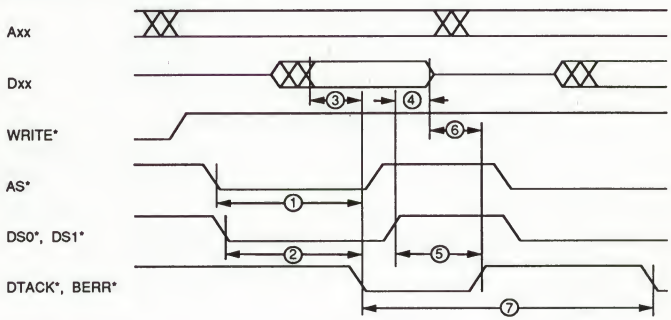



**FIGURE 3-2. VME READ CYCLE TIMING**

| No. | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| 1 | AS* low to DTACK*/BERR* low | 185 | 19Ø | 485 | nsec | 1,3 |
| 2 | DSØ*/DS1* low to DTACK*/BERR* low | 185 | 19Ø | 485 | nsec | 3 |
| 3 | Data valid to DTACK* low | Ø | -- | 3Ø | nsec | -- |
| 4 | DSØ*/DS1* high to data invalid | 1Ø | -- | 4Ø | nsec | -- |
| 5 | DSØ*/DS1* high to DTACK*/BERR* high | 15 | 2Ø | 3Ø | nsec | -- |
| 6 | Data high imp. to DTACK*/BERR* high | Ø | -- | 35 | nsec | -- |
| 7 | DTACK* low to DTACK* low | 23Ø | 245 | 565 | nsec | 2,3 |

Notes:
1) Provided that the VMEbus master drives AS* and DSØ*/DS1* low at the same time.
2) Provided that the VMEbus master drives DSØ*/DS1* low less than 4Ø nsec after receiving DTACK* low.
3) The maximum time can result if a refresh cycle has just started when the board is selected, and a VSB cycle comes before the refresh cycle is finished.

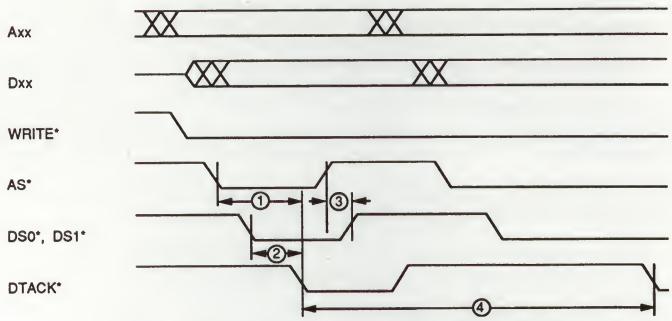



**FIGURE 3-3. VME WRITE CYCLE TIMING**

| No. | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| 1 | AS* low to DTACK* low | 60 | 70 | 355 | nsec | 1,3 |
| 2 | DSØ*/DS1* low to DTACK* low | 60 | 70 | 355 | nsec | 3 |
| 3 | DSØ*/DS1* high to data high | 15 | 20 | 30 | nsec | -- |
| 4 | DTACK* low to DTACK* low | 215 | 230 | 435 | nsec | 2,3 |

Notes:
1) Provided that the VMEbus master drives AS* and DSØ*/DS1* low at the same time.
2) Provided that the VMEbus master drives DSØ*/DS1* low less than 40 nsec after receiving DTACK* low.
3) The maximum time can result if a refresh cycle has just started when the board is selected, and a VSB cycle comes before the refresh cycle is finished.

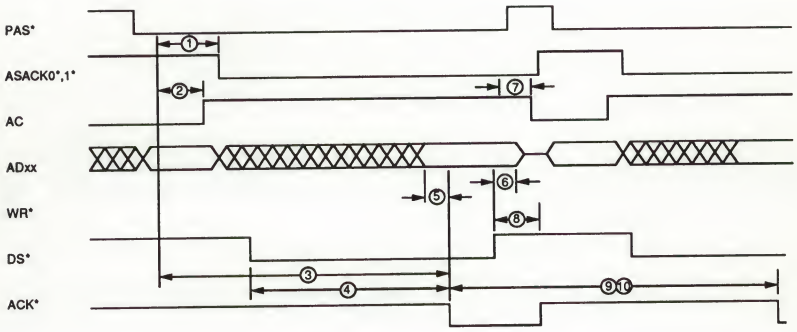



**FIGURE 3-4. VSB READ CYCLE TIMING**

| No. | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| 1 | PAS* low to ASACKØ*/ASACK1* low | 5Ø | 55 | 6Ø | nsec | -- |
| 2 | PAS* low to AC high | 25 | 35 | 45 | nsec | -- |
| 3 | PAS* low to ACK* low | 18Ø | 19Ø | 2ØØ | nsec | 1,2 |
| 4 | DS* low to ACK* low | 18Ø | 19Ø | 2ØØ | nsec | 2,3 |
| 5 | Data valid on bus to ACK* low | 1Ø | 15 | -- | nsec | -- |
| 6 | PAS* high to data three-state on bus | 1Ø | 15 | 2Ø | nsec | -- |
| 7 | PAS* high to AC low | 1Ø | 15 | 2Ø | nsec | -- |
| 8 | PAS* high to ASACKØ*/ASACK1* high | 15 | 2Ø | 25 | nsec | -- |
| 9 | ACK* low to ACK* low | -- | 25Ø | 47Ø | nsec | 2,4,5 |
| 1Ø | ACK* low to ACK* low | -- | 35Ø- | 57Ø | nsec | 2,4,6 |

Notes:
1) With the cache mode jumper J5 not installed, read cycles begin on PAS*. ACK will be stated time or 2Ø nsec after DS* low if PAS* low to DS* low exceeds 17Ø nsec.
2) The maximum time can result if a refresh has just started when the board is selected.
3) With the cache mode jumper J5 installed, read cycles begin on DS*. Time stated in item 4 above applies.
4) Cycle time is dependent on handshakes and speed of master changing from address to data phases. These figures represent DS* low, 75 nsec after PAS* goes low, with ACK* low to DS* high = 1Ø nsec, DS* high to ACK* high = 15 nsec, and ACK* high to PAS* low = 3Ø nsec.
5) These figures are in non-cache mode, with jumper J5 not installed.
6) These figures are in cache mode, with jumper J5 installed.

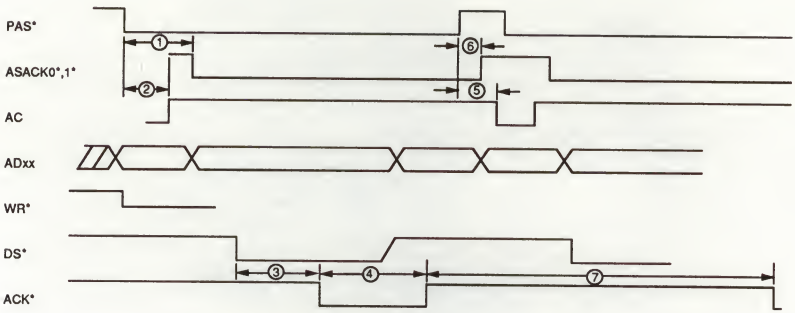



**FIGURE 3-5. VSB WRITE CYCLE TIMING**

| No. | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| 1 | PAS* low to ASACKØ*/ASACK1* low | 5Ø | 55 | 6Ø | nsec | -- |
| 2 | PAS* low to AC high | 25 | 35 | 45 | nsec | -- |
| 3 | DS* low to ACK* low | 6Ø | 75 | 385 | nsec | 1 |
| 4 | DS* high to ACK* high | 1Ø | 2Ø | 3Ø | nsec | -- |
| 5 | PAS* high to AC low | 1Ø | 15 | 2Ø | nsec | -- |
| 6 | PAS* high to ASACKØ*/ASACK1* high | 15 | 2Ø | 25 | nsec | -- |
| 7 | ACK* low to ACK* low | -- | 24Ø | 48Ø | nsec | 1,2 |

Notes:
1) The maximum time can result if a refresh has just started when the board is selected.
2) Cycle time is dependent on handshakes and speed of master changing from address to data phases. These figures represent DS* low, 75 nsec after PAS* goes low, with ACK* low to DS* high = 1Ø nsec, DS* high to ACK* high = 15 nsec, and ACK* high to PAS* low = 3Ø nsec.

### 3.4 VMEbus INTERFACE

The VMEbus interface is one of two ports to the MVME224's DRAM array. The VMEbus interface receives address, data, and control from the VMEbus and provides access to the DRAM array and the Control and Status Register (CSR). It supports byte, word, and longword transfer and unaligned transfers. It responds to 24- or 32-bit addresses with the proper address modifier codes supplied. When responding to 24-bit address codes, the upper eight address lines are not considered. However, the upper eight address mapping

switches must be mapped to Ø (closed). Therefore, with 24-bit addressing, the module cannot be decoded higher than ØØFFFFFF. It supports 16- or 32-bit data transfers. The address modifier codes are decoded in PAL U99, which can be changed to support unique user requirements. It may be mapped to be decoded on any 1-megabyte boundary in the addressing range. It does not support block transfer on the VMEbus.

### 3.5 VSB INTERFACE

The VSB interface is one of two ports to the MVME224's DRAM array. The VSB interface receives address, data and control information from the VSB bus and provides access to the DRAM array. It is a 32-bit address bus and supports byte, word, and longword transfers including unaligned transfers. It does support block transfers up to one megabyte.

### 3.6 CONTROL AND STATUS REGISTER

The Control/Status Register provides a VMEbus accessible register for MVME224 status and control. This register is writable and readable from the VMEbus. The Control/Status Register has three bits which are defined in the following text.

| LDØ7 | LDØ6 | LDØ5 | LDØ4 | LDØ3 | LDØ2 | LDØ1 | LDØØ |
|---|---|---|---|---|---|---|---|
| PES | Not Used | Not Used | Not Used | Not Used | Not Used | WWP | EPD |

**EPD** **< Enable Parity Detection>**

This bit, when set to a "1", allows parity error detection. It is used to enable or disable parity error detection. It is cleared (parity error detection disabled) on power up or reset. It is changed to a "1" when a "1" is written to this bit and cleared to a "Ø" when a "Ø" is written to this bit. When this bit is a "Ø", parity is still written according to the status of the Write Wrong Parity bit.

**WWP** **< Write Wrong Parity>**

This bit, when set to a "1", indicates that a parity error has occurred on this module on either the VMEbus or the VSB. It does not indicate that the last read was a parity error, but that a parity error has occurred since it was last cleared. It is in an undetermined state on power up or reset. It is cleared to a "Ø" when any write occurs to the Control/Status Register and changed to a "1" when a parity error is detected, whether parity is enabled or not.

**PES** **< Parity Error Status>**

This bit, when set to a "1", indicates that a parity error has occurred on this module on either the VMEbus or the VSB. It does not indicate that the last read was a parity error, but that a parity error has occurred since it was last cleared. It is cleared to a "Ø" on power up or reset or when any write occurs to the Control/Status Register and changed to a "1" when a parity error is detected, whether parity is enabled or not.



## 3.7 PARITY

Parity is generated and checked on a byte wide basis. Parity is odd and is checked on each read and reported according to the state of the CSR Parity Enabled bit (bit Ø) in the form of BERR* (VMEbus) or ERR* (VSB bus).

## 3.8 ADDRESS SELECT

Addressing is independently selectable on the VMEbus and VSB bus on 1Mb boundaries. The CSR is mapped dependent on the mapping of the addressing to the RAM on the VMEbus (refer to section 3.9).

When mapping to different addresses on the VMEbus and VSB bus, it must be observed that the RAM on both busses at the same address is the same RAM location, even if they have different starting addresses. For example, if the VMEbus is mapped at ØØØØØØØØ and the VSB bus is mapped at ØØ2ØØØØØ, the RAM at ØØ2ØØØØØ will be the same RAM location on both busses. The RAM location on VME at ØØØØØØØØ is not the same as the RAM location at ØØ2ØØØØØ on the VSB bus. The following table provides the VME/VSB mapping.

**TABLE 3-1. VME/VSB ADDRESS MAPPING**

| S2 -4 | S2 -3 | S2 -2 | S2 -1 | S1 -8 | S1 -7 | S1 -6 | S1 -5 | S1 -4 | S1 -3 | S1 -2 | S1 -1 | VME Address Mapping Switches |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S3 -8 | S3 -7 | S3 -6 | S3 -5 | S3 -4 | S3 -3 | S3 -2 | S3 -1 | S2 -8 | S2 -7 | S2 -6 | S2 -5 | VSB Address Mapping Switches |
| | | | | | | | | | | | | RAM Address In Hexadecimal |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø Ø Ø Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø Ø 1 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | Ø Ø 2 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø Ø 3 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | Ø | Ø Ø 4 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | 1 | Ø Ø 5 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø | Ø Ø 6 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | 1 | Ø Ø 7 Ø Ø Ø Ø Ø |

**TABLE 3-1. VME/VSB ADDRESS MAPPING (cont.)**

| S2 -4 | S2 -3 | S2 -2 | S2 -1 | S1 -8 | S1 -7 | S1 -6 | S1 -5 | S1 -4 | S1 -3 | S1 -2 | S1 -1 | VME Address Mapping Switches |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S3 -8 | S3 -7 | S3 -6 | S3 -5 | S3 -4 | S3 -3 | S3 -2 | S3 -1 | S2 -8 | S2 -7 | S2 -6 | S2 -5 | VSB Address Mapping Switches |
| | | | | | | | | | | | | RAM Address In Hexadecimal |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | Ø | Ø | Ø Ø 8 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | Ø | 1 | Ø Ø 9 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | 1 | Ø | Ø Ø A Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | 1 | 1 | Ø Ø B Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø | Ø | Ø Ø C Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø | 1 | Ø Ø D Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | 1 | Ø | Ø Ø E Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | 1 | 1 | Ø Ø F Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø 1 Ø Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø 1 1 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | Ø 1 2 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø 1 3 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | Ø | Ø 1 4 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | 1 | Ø 1 5 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø | Ø 1 6 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | 1 | Ø 1 7 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø | Ø | Ø | Ø 1 8 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø | Ø | 1 | Ø 1 9 Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø | 1 | Ø | Ø 1 A Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | Ø | 1 | 1 | Ø 1 B Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | 1 | Ø | Ø | Ø 1 C Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | 1 | Ø | 1 | Ø 1 D Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | 1 | 1 | Ø | Ø 1 E Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 | 1 | 1 | 1 | 1 | Ø 1 F Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | Ø | 1 | Ø | Ø | Ø | Ø | Ø | Ø 2 Ø Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | Ø | 1 | Ø | Ø | Ø | Ø | Ø | Ø | Ø 4 Ø Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | Ø | 1 | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø 8 Ø Ø Ø Ø Ø Ø |
| Ø | Ø | Ø | 1 | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 1 Ø Ø Ø Ø Ø Ø Ø |
| Ø | Ø | 1 | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 2 Ø Ø Ø Ø Ø Ø Ø |
| Ø | 1 | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 4 Ø Ø Ø Ø Ø Ø Ø |
| 1 | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | Ø | 8 Ø Ø Ø Ø Ø Ø Ø |

### 3.9 CSR MAPPING

The following table provides the switch settings for the CSR address mapping.

**TABLE 3-2. CSR ADDRESS MAPPING**

| S1 -7 | S1 -6 | S1 -5 | S1 -4 | S1 -3 | S1 -2 | CSR Address | RAM Addresses |
|---|---|---|---|---|---|---|---|
| Ø | Ø | Ø | Ø | Ø | Ø | BEØ1 | XØØXXXXX, XØ1XXXXX, X8ØXXXXX, X81XXXXX |
| Ø | Ø | Ø | Ø | Ø | 1 | BEØ5 | XØ2XXXXX, XØ3XXXXX, X82XXXXX, X83XXXXX |
| Ø | Ø | Ø | Ø | 1 | Ø | BEØ9 | XØ4XXXXX, XØ5XXXXX, X84XXXXX, X85XXXXX |
| Ø | Ø | Ø | Ø | 1 | 1 | BEØD | XØ6XXXXX, XØ7XXXXX, X86XXXXX, X87XXXXX |
| Ø | Ø | Ø | 1 | Ø | Ø | BE11 | XØ8XXXXX, XØ9XXXXX, X88XXXXX, X89XXXXX |
| Ø | Ø | Ø | 1 | Ø | 1 | BE15 | XØAXXXXX, XØBXXXXX, X8AXXXXX, X8BXXXXX |
| Ø | Ø | Ø | 1 | 1 | Ø | BE19 | XØCXXXXX, XØDXXXXX, X8CXXXXX, X8DXXXXX |
| Ø | Ø | Ø | 1 | 1 | 1 | BE1D | XØEXXXXX, XØFXXXXX, X8EXXXXX, X8FXXXXX |
| Ø | Ø | 1 | Ø | Ø | Ø | BE21 | X1ØXXXXX, X11XXXXX, X9ØXXXXX, X91XXXXX |
| Ø | Ø | 1 | Ø | Ø | 1 | BE25 | X12XXXXX, X13XXXXX, X92XXXXX, X93XXXXX |
| Ø | Ø | 1 | Ø | 1 | Ø | BE29 | X14XXXXX, X15XXXXX, X94XXXXX, X95XXXXX |
| Ø | Ø | 1 | Ø | 1 | 1 | BE2D | X16XXXXX, X17XXXXX, X96XXXXX, X97XXXXX |
| Ø | Ø | 1 | 1 | Ø | Ø | BE31 | X18XXXXX, X19XXXXX, X98XXXXX, X99XXXXX |
| Ø | Ø | 1 | 1 | Ø | 1 | BE35 | X1AXXXXX, X1BXXXXX, X9AXXXXX, X9BXXXXX |
| Ø | Ø | 1 | 1 | 1 | Ø | BE39 | X1CXXXXX, X1DXXXXX, X9CXXXXX, X9DXXXXX |
| Ø | Ø | 1 | 1 | 1 | 1 | BE3D | X1EXXXXX, X1FXXXXX, X9EXXXXX, X9FXXXXX |
| Ø | 1 | Ø | Ø | Ø | Ø | BE41 | X2ØXXXXX, X21XXXXX, XAØXXXXX, XA1XXXXX |
| Ø | 1 | Ø | Ø | Ø | 1 | BE45 | X22XXXXX, X23XXXXX, XA2XXXXX, XA3XXXXX |
| Ø | 1 | Ø | Ø | 1 | Ø | BE49 | X24XXXXX, X25XXXXX, XA4XXXXX, XA5XXXXX |
| Ø | 1 | Ø | Ø | 1 | 1 | BE4D | X26XXXXX, X27XXXXX, XA6XXXXX, XA7XXXXX |
| Ø | 1 | Ø | 1 | Ø | Ø | BE51 | X28XXXXX, X29XXXXX, XA8XXXXX, XA9XXXXX |
| Ø | 1 | Ø | 1 | Ø | 1 | BE55 | X2AXXXXX, X2BXXXXX, XAAXXXXX, XABXXXXX |
| Ø | 1 | Ø | 1 | 1 | Ø | BE59 | X2CXXXXX, X2DXXXXX, XACXXXXX, XADXXXXX |
| Ø | 1 | Ø | 1 | 1 | 1 | BE5D | X2EXXXXX, X2FXXXXX, XAEXXXXX, XAFXXXXX |
| Ø | 1 | 1 | Ø | Ø | Ø | BE61 | X3ØXXXXX, X31XXXXX, XBØXXXXX, XB1XXXXX |
| Ø | 1 | 1 | Ø | Ø | 1 | BE65 | X32XXXXX, X33XXXXX, XB2XXXXX, XB3XXXXX |
| Ø | 1 | 1 | Ø | 1 | Ø | BE69 | X34XXXXX, X35XXXXX, XB4XXXXX, XB5XXXXX |
| Ø | 1 | 1 | Ø | 1 | 1 | BE6D | X36XXXXX, X37XXXXX, XB6XXXXX, XB7XXXXX |
| Ø | 1 | 1 | 1 | Ø | Ø | BE71 | X38XXXXX, X39XXXXX, XB8XXXXX, XB9XXXXX |
| Ø | 1 | 1 | 1 | Ø | 1 | BE75 | X3AXXXXX, X3BXXXXX, XBAXXXXX, XBBXXXXX |
| Ø | 1 | 1 | 1 | 1 | Ø | BE79 | X3CXXXXX, X3DXXXXX, XBCXXXXX, XBDXXXXX |
| Ø | 1 | 1 | 1 | 1 | 1 | BE7D | X3EXXXXX, X3FXXXXX, XBEXXXXX, XBFXXXXX |
| 1 | Ø | Ø | Ø | Ø | Ø | BE81 | X4ØXXXXX, X41XXXXX, XCØXXXXX, XC1XXXXX |
| 1 | Ø | Ø | Ø | Ø | 1 | BE85 | X42XXXXX, X43XXXXX, XC2XXXXX, XC3XXXXX |
| 1 | Ø | Ø | Ø | 1 | Ø | BE89 | X44XXXXX, X45XXXXX, XC4XXXXX, XC5XXXXX |

**TABLE 3-2. CSR ADDRESS MAPPING (cont.)**

| S1 -7 | S1 -6 | S1 -5 | S1 -4 | S1 -3 | S1 -2 | CSR Address | RAM Addresses |
|---|---|---|---|---|---|---|---|
| 1 | Ø | Ø | Ø | 1 | 1 | BE8D | X46XXXXX, X47XXXXX, XC6XXXXX, XC7XXXXX |
| 1 | Ø | Ø | 1 | Ø | Ø | BE91 | X48XXXXX, X49XXXXX, XC8XXXXX, XC9XXXXX |
| 1 | Ø | Ø | 1 | Ø | 1 | BE95 | X4AXXXXX, X4BXXXXX, XCAXXXXX, XCBXXXXX |
| 1 | Ø | Ø | 1 | 1 | Ø | BE99 | X4CXXXXX, X4DXXXXX, XCCXXXXX, XCDXXXXX |
| 1 | Ø | Ø | 1 | 1 | 1 | BE9D | X4EXXXXX, X4FXXXXX, XCEXXXXX, XCFXXXXX |
| 1 | Ø | 1 | Ø | Ø | Ø | BEA1 | X5ØXXXXX, X51XXXXX, XDØXXXXX, XD1XXXXX |
| 1 | Ø | 1 | Ø | Ø | 1 | BEA5 | X52XXXXX, X53XXXXX, XD2XXXXX, XD3XXXXX |
| 1 | Ø | 1 | Ø | 1 | Ø | BEA9 | X54XXXXX, X55XXXXX, XD4XXXXX, XD5XXXXX |
| 1 | Ø | 1 | Ø | 1 | 1 | BEAD | X56XXXXX, X57XXXXX, XD6XXXXX, XD7XXXXX |
| 1 | Ø | 1 | 1 | Ø | Ø | BEB1 | X58XXXXX, X59XXXXX, XD8XXXXX, XD9XXXXX |
| 1 | Ø | 1 | 1 | Ø | 1 | BEB5 | X5AXXXXX, X5BXXXXX, XDAXXXXX, XDBXXXXX |
| 1 | Ø | 1 | 1 | 1 | Ø | BEB9 | X5CXXXXX, X5DXXXXX, XDCXXXXX, XDDXXXXX |
| 1 | Ø | 1 | 1 | 1 | 1 | BEBD | X5EXXXXX, X5FXXXXX, XDEXXXXX, XDFXXXXX |
| 1 | 1 | Ø | Ø | Ø | Ø | BEC1 | X6ØXXXXX, X61XXXXX, XEØXXXXX, XE1XXXXX |
| 1 | 1 | Ø | Ø | Ø | 1 | BEC5 | X62XXXXX, X63XXXXX, XE2XXXXX, XE3XXXXX |
| 1 | 1 | Ø | Ø | 1 | Ø | BEC9 | X64XXXXX, X65XXXXX, XE4XXXXX, XE5XXXXX |
| 1 | 1 | Ø | Ø | 1 | 1 | BECD | X66XXXXX, X67XXXXX, XE6XXXXX, XE7XXXXX |
| 1 | 1 | Ø | 1 | Ø | Ø | BED1 | X68XXXXX, X69XXXXX, XE8XXXXX, XE9XXXXX |
| 1 | 1 | Ø | 1 | Ø | 1 | BED5 | X6AXXXXX, X6BXXXXX, XEAXXXXX, XEBXXXXX |
| 1 | 1 | Ø | 1 | 1 | Ø | BED9 | X6CXXXXX, X6DXXXXX, XECXXXXX, XEDXXXXX |
| 1 | 1 | Ø | 1 | 1 | 1 | BEDD | X6EXXXXX, X6FXXXXX, XEEXXXXX, XEFXXXXX |
| 1 | 1 | 1 | Ø | Ø | Ø | BEE1 | X7ØXXXXX, X71XXXXX, XFØXXXXX, XF1XXXXX |
| 1 | 1 | 1 | Ø | Ø | 1 | BEE5 | X72XXXXX, X73XXXXX, XF2XXXXX, XF3XXXXX |
| 1 | 1 | 1 | Ø | 1 | Ø | BEE9 | X74XXXXX, X75XXXXX, XF4XXXXX, XF5XXXXX |
| 1 | 1 | 1 | Ø | 1 | 1 | BEED | X76XXXXX, X77XXXXX, XF6XXXXX, XF7XXXXX |
| 1 | 1 | 1 | 1 | Ø | Ø | BEF1 | X78XXXXX, X79XXXXX, XF8XXXXX, XF9XXXXX |
| 1 | 1 | 1 | 1 | Ø | 1 | BEF5 | X7AXXXXX, X7BXXXXX, XFAXXXXX, XFBXXXXX |
| 1 | 1 | 1 | 1 | 1 | Ø | BEF9 | X7CXXXXX, X7DXXXXX, XFCXXXXX, XFDXXXXX |
| 1 | 1 | 1 | 1 | 1 | 1 | BEFD | X7EXXXXX, X7FXXXXX, XFEXXXXX, XFFXXXXX |

Switch settings Ø = closed, 1 = open.
CSR Addresses are in Short I/O address space.
RAM address - X = don't care.

# CHAPTER 4 - SUPPORT INFORMATION

## 4.1 INTRODUCTION

This chapter provides the connector pin signal descriptions, parts list, parts location diagram, and the schematic diagram for the MVME224-1/-2 memory modules.

## 4.2 INTERCONNECT SIGNALS

The MVME224-1/-2 memory modules use the P1 and P2 backplane connectors to interconnect with VMEbus and to power the board. The P1 and P2 connectors are described in the following sections.

### 4.2.1 P1 Connector

The P1 connector is used to interconnect with the main body of VMEbus signals. It is a standard DIN, triple row, 96-pin male connector. The pin connections, VMEbus signal mnemonics, and signal descriptions for the P1 connector are provided in Table 4-1. Refer to the VMEbus Specification (Rev C.1) for a complete description of the VMEbus signals.

**TABLE 4-1. CONNECTOR P1 INTERCONNECT SIGNALS**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| A1-A8 | DØØ-DØ7 | DATA BUS (bits Ø-7) - Eight of 16 three-state bidirectional data bus signals on P1. |
| A9 | GND | GROUND |
| A1Ø | NC | NOT CONNECTED |
| A11 | GND | GROUND |
| A12 | DS1* | DATA STROBE 1 - A three-state driven signal that enables a data transfer with the slave. It indicates for byte/word transfers that the data transfer will occur on data bus signals DØ8 through D15. |
| A13 | DSØ* | DATA STROBE Ø - A three-state driven signal that enables a data transfer with the slave. It indicates for byte/word transfers that the data transfer will occur on data bus signals DØØ through DØ7. |

**TABLE 4-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| A14 | WRITE* | WRITE ENABLE - A three state driven signal that indicates the data transfer is a write cycle to the slave when asserted, or a read cycle from the slave when not asserted. |
| A15 | GND | GROUND |
| A16 | DTACK* | DATA TRANSFER ACKNOWLEDGE - An open-collector signal driven by the slave. A falling edge indicates that the slave has driven valid data on the data bus during a read cycle, or that the slave has received valid data from the data bus during a write cycle. A low level also indicates the slave may be active on the data bus. |
| A17 | GND | GROUND |
| A18 | AS* | ADDRESS STROBE - A three-state driven signal whose falling edge indicates a valid address is on the address bus. A low level also indicates ownership of VMEbus and the slave resource. |
| A19 | GND | GROUND |
| A20 | IACK* | INTERRUPT ACKNOWLEDGE - A three-state driven signal that indicates an interrupt acknowledge cycle. |
| A21 | IACKIN* | (INTERRUPT) ACKNOWLEDGE INPUT - The IACKIN* and IACKOUT* signals form an interrupt acknowledge daisy-chain to select the interrupting device to supply an interrupt vector. IACKIN* is connected to IACKOUT*. |
| A22 | IACKOUT* | (INTERRUPT) ACKNOWLEDGE OUTPUT - The IACKIN* and IACKOUT* signals form an interrupt acknowledge daisy-chain to select the interrupting device to supply an interrupt vector. IACKOUT* is connected to IACKIN*. |
| A23 | AM4 | ADDRESS MODIFIER (bit 4) - One of six three-state driven signals that specify information about the bus cycle including address size and cycle type. |

**TABLE 4-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| A24-A3Ø | AØ7-AØ1 | ADDRESS BUS (bits 7-1, reverse ordered) - Seven of 23 three-state driven address bus signals on P1. The extended 8 signals of the address bus are on connector P2. |
| A31 | -12V | -12 Vdc POWER |
| A32 | +5V | +5 Vdc POWER |
| B1-BØ3 | NC | NOT CONNECTED |
| B4 | BGØIN* | BUS GRANT Ø IN - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. The remaining three bus-grant-in lines are connected directly to their respective bus-grant-out lines. |
| B5 | BGØOUT* | BUS GRANT Ø OUT - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. The remaining three bus-grant-out lines are connected directly to their respective bus-grant-in lines. |
| B6 | BG1IN* | BUS GRANT 1 IN - Same as BGØIN on pin B4. |
| B7 | BG1OUT* | BUS GRANT 1 OUT - Same as BGØOUT on pin B5. |
| B8 | BG2IN* | BUS GRANT 2 IN - Same as BGØIN on pin B4. |
| B9 | BG2OUT* | BUS GRANT 2 OUT - Same as BGØOUT on pin B5. |
| B1Ø | BG3IN* | BUS GRANT 3 IN - Same as BGØIN on pin B4. |
| B11 | BG3OUT* | BUS GRANT 3 OUT - Same as BGØOUT on pin B5. |
| B12-B15 | BRØ*-BR3* | BUS REQUEST (bits Ø-3) - The bus request lines are open-collector signals generated by requesters. A low level on one of these lines indicates that some master needs to use the DTB. |
| B16-B19 | AMØ-AM3 | ADDRESS MODIFIER (bits Ø-3) - Same as pin A23. |
| B2Ø | GND | GROUND |
| B21,B22 | (reserved) | NOT CONNECTED |
| B23 | GND | GROUND |

**TABLE 4-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| B24-B3Ø | IRQ7*-IRQ1* | INTERRUPT REQUEST (bits 7-1, reverse ordered) - Seven open-collector signals used to request interrupt servicing. |
| B31 | NC | NOT CONNECTED |
| B32 | +5V | +5 Vdc POWER |
| C1-C8 | DØ8-D15 | DATA BUS (bits 8-15) - Same as pins AØ through A8. |
| C9 | GND | GROUND |
| C1Ø | NC | NOT CONNECTED |
| C11 | BERR* | BUS ERROR - An active low output signal that indicates an error has occurred during a data transfer cycle. |
| C12 | SYSRESET* | SYSTEM RESET - An open-collector signal which, when low, causes the system to be reset. |
| C13 | LWORD* | LONGWORD - A three-state driven signal that indicates the data transfer is a longword (32-bit transfer) aligned operation. When not asserted, it indicates a byte or word operation. |
| C14 | AM5 | ADDRESS MODIFIER 5 - Same as AM4 on pin A23. |
| C15-C3Ø | A23-AØ8 | ADDRESS BUS (bits 23-Ø8, reverse ordered) - Sixteen of 23 three-state driven address bus signals on P1. The extended 8 signals of the address bus are on connector P2. |
| C31 | NC | NOT CONNECTED |
| C32 | +5V | +5 Vdc POWER |

### 4.2.2 P2 Connector

The P2 connector is used to interconnect with the extended sections of the address and data busses on the VMEbus, the VSB bus, and to additional power and ground pins. Connector P2 is a standard DIN, triple row, 96-pin male connector. Table 4-2 provides the pin connections, signal mnemonics, and signal descriptions. Refer to the VMEbus Specification (Rev C.1) for a complete description of VMEbus signals.

**TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| A1 | AD00 | (VSB) ADDRESS/DATA BUS (bit 00) - One of 32 multiplexed address/data lines that are controlled by the three-state drivers on the master and slave devices. These lines are all active high, TTL three-state signals. |
| A2 | AD02 | (VSB) ADDRESS/DATA BUS (bit 02) - Same as AD00 on pin A1. |
| A3 | AD04 | (VSB) ADDRESS/DATA BUS (bit 04) - Same as AD00 on pin A1. |
| A4 | AD06 | (VSB) ADDRESS/DATA BUS (bit 06) - Same as AD00 on pin A1. |
| A5 | AD08 | (VSB) ADDRESS/DATA BUS (bit 08) - Same as AD00 on pin A1. |
| A6 | AD10 | (VSB) ADDRESS/DATA BUS (bit 10) - Same as AD00 on pin A1. |
| A7 | AD12 | (VSB) ADDRESS/DATA BUS (bit 12) - Same as AD00 on pin A1. |
| A8 | AD14 | (VSB) ADDRESS/DATA BUS (bit 14) - Same as AD00 on pin A1. |
| A9 | AD16 | (VSB) ADDRESS/DATA BUS (bit 16) - Same as AD00 on pin A1. |
| A10 | AD18 | (VSB) ADDRESS/DATA BUS (bit 18) - Same as AD00 on pin A1. |

**TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| A11 | AD2Ø | (VSB) ADDRESS/DATA BUS (bit 2Ø) - Same as ADØØ on pin A1. |
| A12 | AD22 | (VSB) ADDRESS/DATA BUS (bit 22) - Same as ADØØ on pin A1. |
| A13 | AD24 | (VSB) ADDRESS/DATA BUS (bit 24) - Same as ADØØ on pin A1. |
| A14 | AD26 | (VSB) ADDRESS/DATA BUS (bit 26) - Same as ADØØ on pin A1. |
| A15 | AD28 | (VSB) ADDRESS/DATA BUS (bit 28) - Same as ADØØ on pin A1. |
| A16 | AD3Ø | (VSB) ADDRESS/DATA BUS (bit 3Ø) - Same as ADØØ on pin A1. |
| A17 | GND | GROUND |
| A18 | NC | NOT CONNECTED |
| A19 | DS* | (VSB) DATA STROBE - The falling edge of DS* indicates that a valid data transfer will occur over ADØØ through AD31. During write cycles, write data is valid at the falling edge of DS*. This line is an active low, TTL three-state signal. |
| A2Ø | WR* | (VSB) WRITE - This signal, when low, indicates that a write operation is to be performed and when high, indicates that a read operation will occur. WR* is valid when AS* is asserted on the bus. Line WR* is a TTL, three-state signal. |
| A21 | SPACEØ | SPACE SELECT (bit Ø) - One of two lines that are driven by the active master with a space code. They are used to select one of three address spaces, or to initiate an (interrupt) ACK* or an arbitration cycle. |
| A22 | SPACE1 | SPACE SELECT (bit 1) - Same as SPACEØ on pin A21. |

**TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| A23 | LOCK | (VSB) BUS LOCK - This signal, when low, indicates the bus is locked and that no other master can obtain possession of the bus. LOCK* is also used in certain modes to indicate that a block transfer cycle is in progress. LOCK* is an active low, TTL three-state signal. |
| A24 | ERR* | (VSB) BUS ERROR - This signal, when low, is issued by the selected slave module to indicate a fault condition while attempting a data transfer operation. This would typically be the result of a parity error detected on a slave device. Line ERR* is an active low, TTL open-collector signal. |
| A25-A27 | GND | GROUND |
| A28-A30 | NC | NOT CONNECTED |
| A31 | BGIN* | (VSB) BUS GRANT IN - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. Connected directly to BGOUT*. |
| A32 | NC | NOT CONNECTED |
| B1 | +5V | +5 Vdc POWER |
| B2 | GND | GROUND |
| B3 | VMELOCK* | VMEbus LOCK - This signal, when low, indicates that the bus is in the middle of a multiple-cycle access and that any other bus should be excluded from shared memory. |
| B4-B11 | A24-A31 | ADDRESS BUS (bits 24-31) - Eight three-state driven address bus signals that form the extended section of the address bus. The standard 23 signals of the address bus are on connector P1. |
| B12 | GND | GROUND |
| B13 | +5V | +5 Vdc POWER |

**TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| B14-B21 | D16-D23 | DATA BUS (bits 17-23) - Eight of 16 bidirectional three-state driven data lines which provide the expanded data path between the data transfer bus master and slave. |
| B22 | GND | GROUND |
| B23-B3Ø | D24-D31 | DATA BUS (bits 24-31) - Same as D16 through D23 on pins B14 through B21. |
| B31 | GND | GROUND |
| B32 | +5V | +5 Vdc POWER |
| C1 | ADØ1 | (VSB) ADDRESS/DATA BUS (bit Ø1) - Same as ADØØ on pin A1. |
| C2 | ADØ3 | (VSB) ADDRESS/DATA BUS (bit Ø3) - Same as ADØØ on pin A1. |
| C3 | ADØ5 | (VSB) ADDRESS/DATA BUS (bit Ø5) - Same as ADØØ on pin A1. |
| C4 | ADØ7 | (VSB) ADDRESS/DATA BUS (bit Ø7) - Same as ADØØ on pin A1. |
| C5 | ADØ9 | (VSB) ADDRESS/DATA BUS (bit Ø9) - Same as ADØØ on pin A1. |
| C6 | AD11 | (VSB) ADDRESS/DATA BUS (bit 11) - Same as ADØØ on pin A1. |
| C7 | AD13 | (VSB) ADDRESS/DATA BUS (bit 13) - Same as ADØØ on pin A1. |
| C8 | AD15 | (VSB) ADDRESS/DATA BUS (bit 15) - Same as ADØØ on pin A1. |
| C9 | AD17 | (VSB) ADDRESS/DATA BUS (bit 17) - Same as ADØØ on pin A1. |
| C1Ø | AD19 | (VSB) ADDRESS/DATA BUS (bit 19) - Same as ADØØ on pin A1. |

**TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| C11 | AD21 | (VSB) ADDRESS/DATA BUS (bit 21) - Same as AD00 on pin A1. |
| C12 | AD23 | (VSB) ADDRESS/DATA BUS (bit 23) - Same as AD00 on pin A1. |
| C13 | AD25 | (VSB) ADDRESS/DATA BUS (bit 25) - Same as AD00 on pin A1. |
| C14 | AD27 | (VSB) ADDRESS/DATA BUS (bit 27) - Same as AD00 on pin A1. |
| C15 | AD29 | (VSB) ADDRESS/DATA BUS (bit 29) - Same as AD00 on pin A1. |
| C16 | AD31 | (VSB) ADDRESS/DATA BUS (bit 31) - Same as AD00 on pin A1. |
| C17-C20 | GND | GROUND |
| C21 | SIZE0* | (VSB) BUS SIZE (bit 0) - One of two lines that in conjunction with address A00, determines the active portion of the data bus. This line is an active low, TTL three-state signal. |
| C22 | PAS* | (VSB) ADDRESS STROBE - The falling edge of PAS* indicates that a valid address is present on the AD00 through AD31 bus. This line is an active low, TTL three-state signal. |
| C23 | SIZE1* | (VSB) BUS SIZE (bit 1) - Same as SIZE0 on pin C21. |
| C24 | GND | GROUND |
| C25 | ACK* | (VSB) DATA TRANSFER ACKNOWLEDGE - This signal is issued by a slave device to complete the handshake for a data transfer operation. This line is an active low, TTL open-collector signal. |
| C26 | AC | (VSB) ADDRESS DECODE COMPLETE - This signal is issued by a slave device to indicate that address decoding has been completed. All slave devices must allow AC (Address Decode Complete) to go high after the decode interval has elapsed regardless |

**TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| | | whether the device is selected by the current address on the bus. This line is an active high, TTL open-collector signal. |
| C27 | ASACK1* | (VSB) ADDRESS/SIZE ACKNOWLEDGE (bit 1) - One of two lines that are driven by the VSB slave devices and are used to perform several functions. The slave device that is selected by the address decoding must drive at least one ASACK* signal to control switching the multiplexed address/data bus from address to data. Secondly, both are encoded to indicate to the master the size of the data bus for the slave module. Finally, ASACK* can be gated with the signal AC (Address Decode Complete) on the master device. The condition of AC active and ASACK* inactive, while AS* is asserted, is defined to indicate that no VSB slave module has decoded the address being driven at that time, or that there are no VSB slave modules installed. This provides the VSB master the opportunity to switch to the VMEbus when VSB slaves are not responding. ASACKØ* and ASACK1* are active low, TTL open-collector signals. |
| C28 | ASACKØ* | (VSB) ADDRESS/SIZE ACKNOWLEDGE (bit Ø) - Same as ASACK1* on pin C27. |
| C29 | CACHE* | (VSB) CACHEABLE - CACHE* is issued by a slave device at the same time that ASACKØ* and ASACK1* are issued to indicate that the current transfer is cacheable. CACHE* remains inactive to indicate that the transfer is non-cacheable. This line is an active low, TTL open-collector signal. |
| C3Ø | WAIT* | (VSB) HOLD THIS CYCLE - This signal is an output line used in conjunction with the signals AC. If this line is driven low at the beginning of a cycle, addresses must remain stable and DS* cannot be driven until AC goes high. Also, data must remain valid along with DS* during the data transfer portion of the cycle until WAIT* is negated. This signal is an active low TTL open-collector signal. |

**TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)**

| Pin Number | Signal Mnemonic | Signal Name and Description |
|---|---|---|
| C31 | NC | NOT CONNECTED (on MVME224). |
| C32 | BGOUT* | (VSB) BUS GRANT OUT - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. Connected directly to BGIN*. |

## 4.3 PARTS LIST

The parts location diagram for the MVME224 is provided in Figure 4-1. The reference designation, part number, and description for each component are listed in Table 4-3. This parts list reflects the latest issue of the MVME224 hardware at the time of the release of this user's manual.

**TABLE 4-3. MVME224 PARTS LIST**

| Reference Designation | Motorola Part Number | Description |
|---|---|---|
| -- | 84-W85ØØBØ1B | Printed wiring board assembly, MVME224-2 |
| C1-1Ø, C13-21, C24-37, C4Ø-51 | 21NW9632AØ3 | Capacitor, ceramic, axial, .1MF, 5Ø Vdc |
| C11 | 21NW96Ø4A58 | Capacitor, ceramic, radial, 33ØpF, 5Ø Vdc |
| C12 | 21SW992CØ14 | Capacitor, ceramic, .Ø1ØMF, 5Ø Vdc |
| C22,C23, C38,C39 | 23NW9618A82 | Capacitor, electrolytic, radial, 22MF, 25 Vdc |
| DL1 | Ø1NW98Ø4C8Ø | Delay module, 1ØØ nsec |
| DL2 | Ø1NW98Ø4C33 | Delay module, 4Ø nsec |
| DL3 | 51NW9615W26 | IC, DS1ØØØM-1ØØ |
| DL4-6 | 51NW9615W46 | IC, DS1ØØØM-5Ø |
| DS1,DS2 | 48NW9612A59 | LED, green, right-angle |
| J1,J3 | 29NW98Ø5B44 | Jumper, 2-pin (2 req'd)[used at J1(1-2),J3(1-2)] |
| J2 | 29NW98Ø5CØ7 | Pin, Ø.Ø25-inch square, gold, autoinsert (6 req'd)[used at J2(1-2),J4(1-2),J5(1-2)] |
| P1,P2 | 28NW98Ø2E51 | Connector, 96-pin, plug, PWB |
| -- | Ø5NW9ØØ7A26 | Eyelet, Ø.Ø89-inch OD x Ø.344-inch long (4 req'd)(used with P1 and P2) |
| R1,R2 | Ø6SW-124A29 | Resistor, film, 1/8W, 5%, 15Ø ohms |

**TABLE 4-3. MVME224 PARTS LIST (cont.)**

| Reference Designation | Motorola Part Number | Description |
|---|---|---|
| R3,R4,R7, R8,R1Ø | 51NW9626A37 | Resistor network, SIP, four 33 ohms **(for MVME224-1 version only)** |
| R3,R4, R7-R1Ø, R12-14 | 51NW9626A37 | Resistor network, SIP, four 33 ohms **(for MVME224-2 version only)** |
| R5 | 51NW9626A49 | Resistor network, SIP, seven 1ØK ohms |
| R6,R15, R16-21 | 51NW9626B56 | Resistor network, SIP, nine 1ØK ohms |
| R11 | Ø6SW-124A81 | Resistor, film, 1/8W, 5%, 22K ohms |
| R22 | 51NW9626B47 | Resistor network, SIP, nine 22K ohms |
| S1-3 | 4ØNW98Ø1A34 | Switch, DIP, SPST, 8-position |
| U1 | 51NW9615K47 | IC, 74F244PC |
| U2-19, U27-44 | 51NW9615U44 | IC, M5M4C1ØØØL-1Ø **(for MVME224-1 version only)** |
| U2-19, U27-44, U52-69, U76-93 | 51NW9615U44 | IC, M5M4C1ØØØL-1Ø **(for MVME224-2 version only)** |
| U2Ø,U45, U7Ø | 51NW9615K6Ø | IC, 74F158APC |
| U23,U24 U122,U123, U134,U135, U148,U149 | 51NW9615R36 | IC, 74F543SPC |
| U25 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U25) |
| U26 | (NOTE) | IC, programmed **(for MVME224-1 version only)** |

**TABLE 4-3. MVME224 PARTS LIST (cont.)**

| Reference Designation | Motorola Part Number | Description |
|---|---|---|
| U26 | (NOTE) | IC, programmed **(for MVME224-2 version only)** |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U26) |
| U46 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U46) |
| U47 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U47) |
| U48 | (NOTE) | IC, programmed |
| -- | Ø9NW9811A78 | Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U48) |
| U49,U74, U75,U121, U132,U133 | 51NW9615K99 | IC, 74F374PC |
| U5Ø | 51NW9615B65 | IC, MC1455P1 |
| U72 | (NOTE) | IC, programmed |
| -- | Ø9NW9811A78 | Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U72) |
| U73 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U73) |
| U95,U145, U146 | 51NW9615F85 | IC, SN74S38N |
| U96 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U96) |

**TABLE 4-3. MVME224 PARTS LIST (cont.)**

| Reference Designation | Motorola Part Number | Description |
|---|---|---|
| U97 | (NOTE) | IC, programmed (for MVME224-1 version only) |
| U97 | (NOTE) | IC, programmed (for MVME224-2 version only) |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U97) |
| U98 | (NOTE) | IC, programmed (for MVME224-1 version only) |
| U98 | (NOTE) | IC, programmed (for MVME224-2 version only) |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U98) |
| U99 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U99) |
| UlØØ | 51NW9615R16 | IC, SN74ALSØ4AN |
| UlØ1 | (NOTE) | IC, programmed (for MVME224-1 version only) |
| UlØ1 | (NOTE) | IC, programmed (for MVME224-2 version only) |
| -- | Ø9NW9811A78 | Socket, IC, DIL, 2Ø-pin (1 req'd)(used at UlØ1) |
| UlØ2,UlØ4 | 51NW9615K18 | IC, 74F373PC |
| UlØ3,UlØ5 | 51NW9615W31 | IC, SN74AS841NT |
| UlØ6,UlØ7 | 51NW9615M9Ø | IC, 74F245PC |
| UlØ8,UlØ9, Ul19,Ul2Ø | 51NW9615V91 | IC, SN74AS28ØN |
| Ul1Ø | 51NW9615K65 | IC, 74F64PC |

**TABLE 4-3. MVME224 PARTS LIST (cont.)**

| Reference Designation | Motorola Part Number | Description |
|---|---|---|
| U111 | 51NW9615K66 | IC, 74F32PC |
| U112 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U112) |
| U113 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U113) |
| U114 | (NOTE) | IC, programmed |
| -- | Ø9NW9811A78 | Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U114) |
| U115 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U115) |
| U116 | (NOTE) | IC, programmed |
| -- | Ø9NW9811A78 | Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U116) |
| U117 | (NOTE) | IC, programmed |
| -- | Ø9NW9811A78 | Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U117) |
| U118 | (NOTE) | IC, programmed |
| -- | Ø9NW9811A78 | Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U118) |
| U124 | 51NW9615K71 | IC, 74FØ4PC |
| U125 | 51NW9615K67 | IC, 74F2ØPC |
| U126-13Ø, U138 | 51NW9615J39 | IC, 74F74PC |

**TABLE 4-3. MVME224 PARTS LIST (cont.)**

| Reference Designation | Motorola Part Number | Description |
|---|---|---|
| U131 | (NOTE) | IC, programmed (for MVME224-1 version only) |
| U131 | (NOTE) | IC, programmed (for MVME224-2 version only) |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U131) |
| U136 | 51NW9615K7Ø | IC, 74FØ8PC |
| U137 | 51NW9615K73 | IC, 74FØØPC |
| U139 | (NOTE) | IC, programmed |
| -- | Ø9-W4659B12 | Socket, IC, SIL, 12-pin (2 req'd)(used at U139) |
| U14Ø | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U14Ø) |
| U141 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U141) |
| U142 | (NOTE) | IC, programmed (for MVME224-1 version only) |
| U142 | (NOTE) | IC, programmed (for MVME224-2 version only) |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U142) |
| U143 | (NOTE) | IC, programmed |
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U143) |
| U144 | (NOTE) | IC, programmed |

**TABLE 4-3. MVME224 PARTS LIST (cont.)**

| Reference Designation | Motorola Part Number | Description |
|---|---|---|
| -- | Ø9NW9811BØ1 | Socket, IC, DIL, 24-pin (1 req'd)(used at U144) |
| U147 | (NOTE) | IC, programmed |
| -- | Ø9-W4659B1Ø | Socket, IC, SIL, 1Ø-pin (2 req'd)(used at U147) |
| -- | 67NW9415A17 | Kit, ejector handle, 6U component |
| -- | 64-W55Ø1BØ1A | Panel, front, MVME224-1,2 |
| -- | 33-W5Ø89BØ1 | Nameplate, Scanbe, logo |
| -- | 33-W5478BØ1 | Nameplate, MVME224-1 (for MVME224-1 version only) |
| -- | 33-W5537BØ1 | Nameplate, MVME224-2 (for MVME224-2 version only) |
| -- | 42NW94Ø1B14 | Captive collar screw (2 req'd) |
| -- | Ø3NW9ØØ4B48 | Screw, captive, M2.5 (2 req'd) |

NOTE: When ordering, use the number labeled on the part.

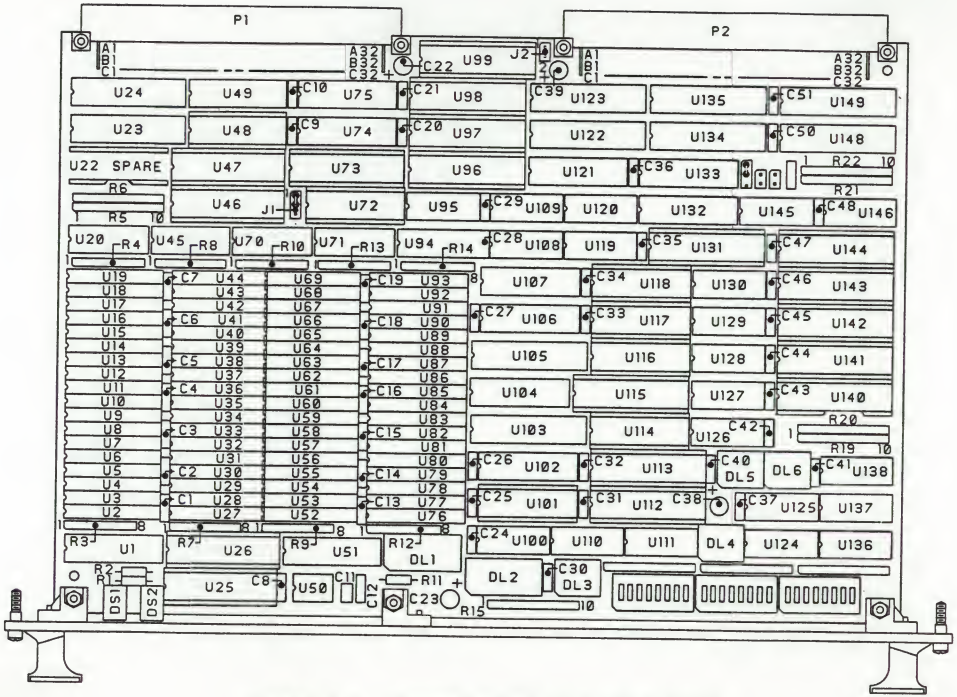



FIGURE 4-1. MVME224 PARTS LOCATION DIAGRAM

## 4.4 SCHEMATIC DIAGRAMS

Figure 4-2 (25 sheets) contains detailed schematic diagrams of the internal circuitry comprising the MVME224. These schematic diagrams represent the lastest design. Occasionally, minor component changes are made at the factory. Therefore, when replacing a component, always use the same value as the defective component even though the schematic diagram may indicate a different value or type.

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3500B_, CURRENT REVISION / CONFIGURATION APPLIES.
2. UNLESS OTHERWISE SPECIFIED.
   ALL RESISTORS ARE IN OHMS, ±5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   [ DENOTES - ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING, FOR FULL PART TYPE, REFER TO TABLE 1.
8. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:

   SHEET — 6 A6 — ZONE

9. COMPONENTS INSTALLED ON B02 (8 MEGABYTE) VERSION ONLY.

| | |
|---|---|
| U149 | U21,U22 |
| S3 | |
| R22 | |
| P2 | |
| J5 | J3 |
| DS2 | |
| DL6 | |
| C51 | |
| HIGHEST NUMBER USED | NOT USED |
| REFERENCE DESIGNATIONS | |

7 6 5 4 3

TABLE 1

| REF DES | TYPE 4 | GND | +5V | SH |
|---|---|---|---|---|
| DL1 | 100NS | 7 | 14 | 14 |
| DL2 | 40NS | 7 | 14 | 14 |
| DL3 | 100NS | 4 | 8 | 14 |
| DL4 | 50NS | 4 | 8 | 10 |
| DL5 | 50NS | 4 | 8 | 7 |
| DL6 | 50NS | 4 | 8 | 10 |
| U1 | 74F244 | 10 | 20 | 14 |
| U2 | M5M4C1000L | 4 | 15 | 25 |
| U3 | M5M4C1000L | 4 | 15 | 25 |
| U4 | M5M4C1000L | 4 | 15 | 22 |
| U5 | M5M4C1000L | 4 | 15 | 22 |
| U6 | M5M4C1000L | 4 | 15 | 22 |
| U7 | M5M4C1000L | 4 | 15 | 22 |
| U8 | M5M4C1000L | 4 | 15 | 22 |
| U9 | M5M4C1000L | 4 | 15 | 22 |
| U10 | M5M4C1000L | 4 | 15 | 22 |
| U11 | M5M4C1000L | 4 | 15 | 22 |
| U12 | M5M4C1000L | 4 | 15 | 21 |
| U13 | M5M4C1000L | 4 | 15 | 21 |
| U14 | M5M4C1000L | 4 | 15 | 21 |
| U15 | M5M4C1000L | 4 | 15 | 21 |
| U16 | M5M4C1000L | 4 | 15 | 21 |
| U17 | M5M4C1000L | 4 | 15 | 21 |
| U18 | M5M4C1000L | 4 | 15 | 21 |
| U19 | M5M4C1000L | 4 | 15 | 21 |
| U20 | 74F158 | 8 | 16 | 18 |
| U23 | 74F543 | 12 | 24 | 6 |
| U24 | 74F543 | 12 | 24 | 6 |
| U25 | PAL20L8 | 12 | 24 | 14 |
| U26 | PAL20L8 | 12 | 24 | 14 |
| U27 | M5M4C1000L | 4 | 15 | 25 |
| U28 | M5M4C1000L | 4 | 15 | 25 |
| U29 | M5M4C1000L | 4 | 15 | 22 |
| U30 | M5M4C1000L | 4 | 15 | 22 |
| U31 | M5M4C1000L | 4 | 15 | 22 |
| U32 | M5M4C1000L | 4 | 15 | 22 |
| U33 | M5M4C1000L | 4 | 15 | 22 |
| U34 | M5M4C1000L | 4 | 15 | 22 |
| U35 | M5M4C1000L | 4 | 15 | 22 |
| U36 | M5M4C1000L | 4 | 15 | 22 |
| U37 | M5M4C1000L | 4 | 15 | 21 |
| U38 | M5M4C1000L | 4 | 15 | 21 |
| U39 | M5M4C1000L | 4 | 15 | 21 |
| U40 | M5M4C1000L | 4 | 15 | 21 |
| U41 | M5M4C1000L | 4 | 15 | 21 |
| U42 | M5M4C1000L | 4 | 15 | 21 |
| U43 | M5M4C1000L | 4 | 15 | 21 |
| U44 | M5M4C1000L | 4 | 15 | 21 |
| U45 | 74F158 | 8 | 16 | 18 |
| U46 | PAL22V10 | 12 | 24 | 17 |
| U47 | PAL22V10 | 12 | 24 | 17 |
| U48 | PAL16L8 | 10 | 20 | 7 |
| U49 | 74F374 | 10 | 20 | 7 |
| U50 | MC1455 | 1 | 8 | 13 |
| U51 | 74F244 | 10 | 20 | 14 |
| U52 | M5M4C1000L | 4 | 15 | 25 |
| U53 | M5M4C1000L | 4 | 15 | 25 |
| U54 | M5M4C1000L | 4 | 15 | 24 |

TABLE 1 CONT

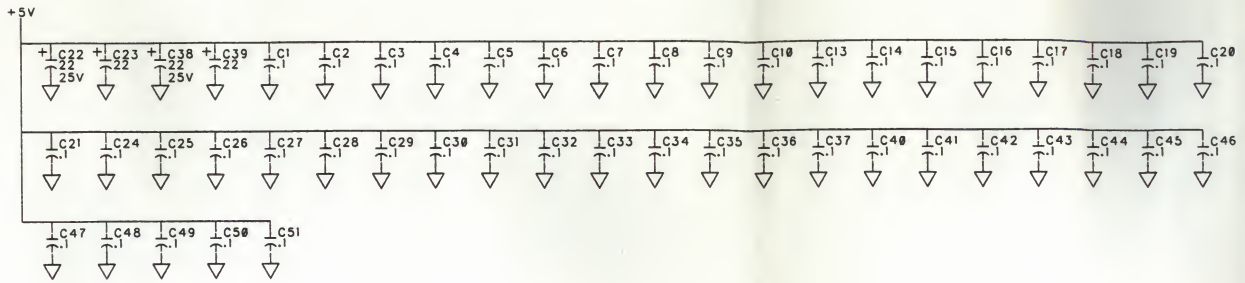
| REF DES | TYPE 4 | GND | +5V | SH |
|---|---|---|---|---|
| U55 | M5M4C1000L | 4 | 15 | 24 |
| U56 | M5M4C1000L | 4 | 15 | 24 |
| U57 | M5M4C1000L | 4 | 15 | 24 |
| U58 | M5M4C1000L | 4 | 15 | 24 |
| U59 | M5M4C1000L | 4 | 15 | 24 |
| U60 | M5M4C1000L | 4 | 15 | 24 |
| U61 | M5M4C1000L | 4 | 15 | 24 |
| U62 | M5M4C1000L | 4 | 15 | 23 |
| U63 | M5M4C1000L | 4 | 15 | 23 |
| U64 | M5M4C1000L | 4 | 15 | 23 |
| U65 | M5M4C1000L | 4 | 15 | 23 |
| U66 | M5M4C1000L | 4 | 15 | 23 |
| U67 | M5M4C1000L | 4 | 15 | 23 |
| U68 | M5M4C1000L | 4 | 15 | 23 |
| U69 | M5M4C1000L | 4 | 15 | 23 |
| U70 | 74F158 | 8 | 16 | 18 |
| U71 | 74F158 | 8 | 16 | 18 |
| U72 | PAL16L8 | 10 | 20 | 17 |
| U73 | PAL22V10 | 12 | 24 | 17 |
| U74 | 74F374 | 10 | 20 | 7 |
| U75 | 74F374 | 10 | 20 | 7 |
| U76 | M5M4C1000L | 4 | 15 | 25 |
| U77 | M5M4C1000L | 4 | 15 | 25 |
| U78 | M5M4C1000L | 4 | 15 | 24 |
| U79 | M5M4C1000L | 4 | 15 | 24 |
| U80 | M5M4C1000L | 4 | 15 | 24 |
| U81 | M5M4C1000L | 4 | 15 | 24 |
| U82 | M5M4C1000L | 4 | 15 | 24 |
| U83 | M5M4C1000L | 4 | 15 | 24 |
| U84 | M5M4C1000L | 4 | 15 | 24 |
| U85 | M5M4C1000L | 4 | 15 | 24 |
| U86 | M5M4C1000L | 4 | 15 | 23 |
| U87 | M5M4C1000L | 4 | 15 | 23 |
| U88 | M5M4C1000L | 4 | 15 | 23 |
| U89 | M5M4C1000L | 4 | 15 | 23 |
| U90 | M5M4C1000L | 4 | 15 | 23 |
| U91 | M5M4C1000L | 4 | 15 | 23 |
| U92 | M5M4C1000L | 4 | 15 | 23 |
| U93 | M5M4C1000L | 4 | 15 | 23 |
| U94 | 74F158 | 8 | 16 | 18 |
| U95 | 74S38 | 7 | 14 | 2,6 |
| U96 | PAL22V10 | 12 | 24 | 8 |
| U97 | PAL22V10 | 12 | 24 | 8 |
| U98 | PAL22V10 | 12 | 24 | 8 |
| U99 | PAL22V10 | 12 | 24 | 8 |
| U100 | 74ALS04 | 7 | 14 | 2,12,13 |
| U101 | PAL16L8 | 10 | 20 | 16 |
| U102 | 74F373 | 10 | 20 | 20 |
| U103 | 74AS841 | 12 | 24 | 20 |
| U104 | 74F373 | 10 | 20 | 20 |
| U105 | 74AS841 | 12 | 24 | 20 |
| U106 | 74F245 | 10 | 20 | 12 |
| U107 | 74F245 | 10 | 20 | 12 |
| U108 | 74AS280 | 7 | 14 | 19 |
| U109 | 74AS280 | 7 | 14 | 19 |
| U110 | 74F64 | 7 | 14 | 19 |
| U111 | 74F32 | 7 | 14 | 2,14 |
| U112 | PAL22V10 | 12 | 24 | 16 |
| U113 | PAL20L8 | 12 | 24 | 16 |
| U114 | PAL16L8 | 10 | 20 | 16 |

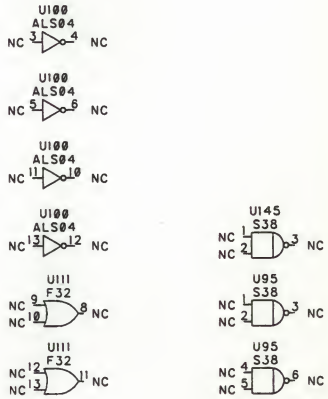
TABLE 1 CONT

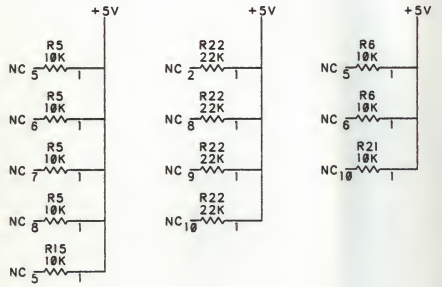
| REF DES | TYPE 4 | GND | +5V | SH |
|---|---|---|---|---|
| U115 | PAL20L8 | 12 | 24 | 17 |
| U116 | PAL16L8 | 10 | 20 | 15 |
| U117 | PAL16R6 | 10 | 20 | 15 |
| U118 | PAL16L8 | 10 | 20 | 19 |
| U119 | 74AS280 | 7 | 14 | 19 |
| U120 | 74AS280 | 7 | 14 | 19 |
| U121 | 74F374 | 10 | 20 | 10 |
| U122 | 74F543 | 12 | 24 | 9 |
| U123 | 74F543 | 12 | 24 | 9 |
| U124 | 74F04 | 7 | 14 | 6,10,14 |
| U125 | 74F20 | 7 | 14 | 7,10 |
| U126 | 74F74 | 7 | 14 | 13,17 |
| U127 | 74F74 | 7 | 14 | 15 |
| U128 | 74F74 | 7 | 14 | 15 |
| U129 | 74F74 | 7 | 14 | 15 |
| U130 | 74F74 | 7 | 14 | 9 |
| U131 | PAL22V10 | 12 | 24 | 11 |
| U132 | 74F374 | 10 | 20 | 10 |
| U133 | 74F374 | 10 | 20 | 10 |
| U134 | 74F543 | 12 | 24 | 9 |
| U135 | 74F543 | 12 | 24 | 9 |
| U136 | 74F08 | 7 | 14 | 6,9,10,17 |
| U137 | 74F00 | 7 | 14 | 9,14 |
| U138 | 74F74 | 7 | 14 | 6 |
| U139 | PAL20RA10 | 12 | 24 | 13 |
| U140 | PAL20L8 | 12 | 24 | 6 |
| U141 | PAL20L8 | 12 | 24 | 9 |
| U142 | PAL22V10 | 12 | 24 | 11 |
| U143 | PAL22V10 | 12 | 24 | 11 |
| U144 | PAL22V10 | 12 | 24 | 11 |
| U145 | 74S38 | 7 | 14 | 2,9 |
| U146 | 74S38 | 7 | 14 | 9,10 |
| U147 | PAL16L8 | 10 | 20 | 10 |
| U148 | 74F543 | 12 | 24 | 6 |
| U149 | 74F543 | 12 | 24 | 6 |



**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 1 OF 25)**



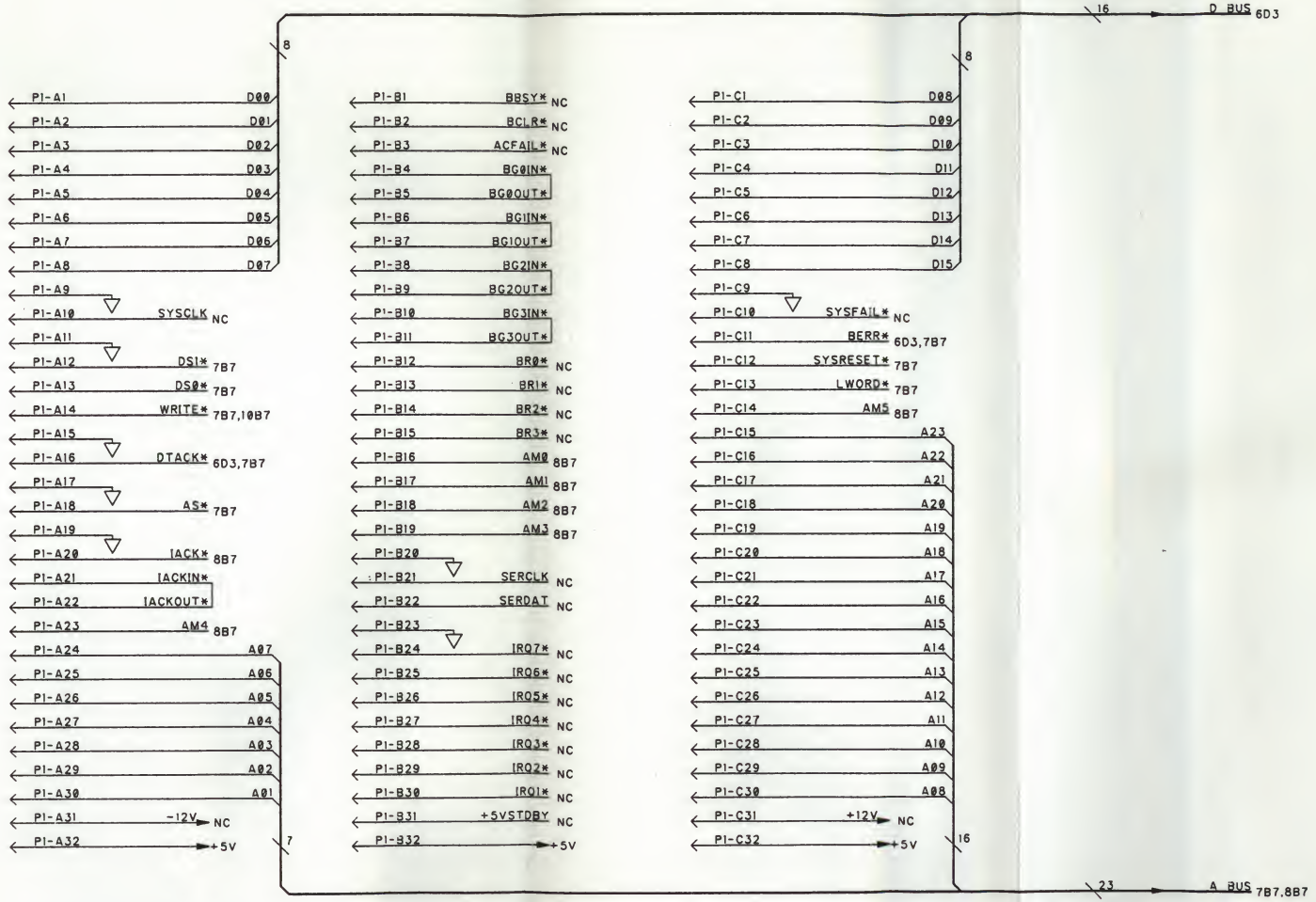




NOT USED

SPARES AND BYPASS CAPS
63DW3500B0C REV E SH 2 OF 25

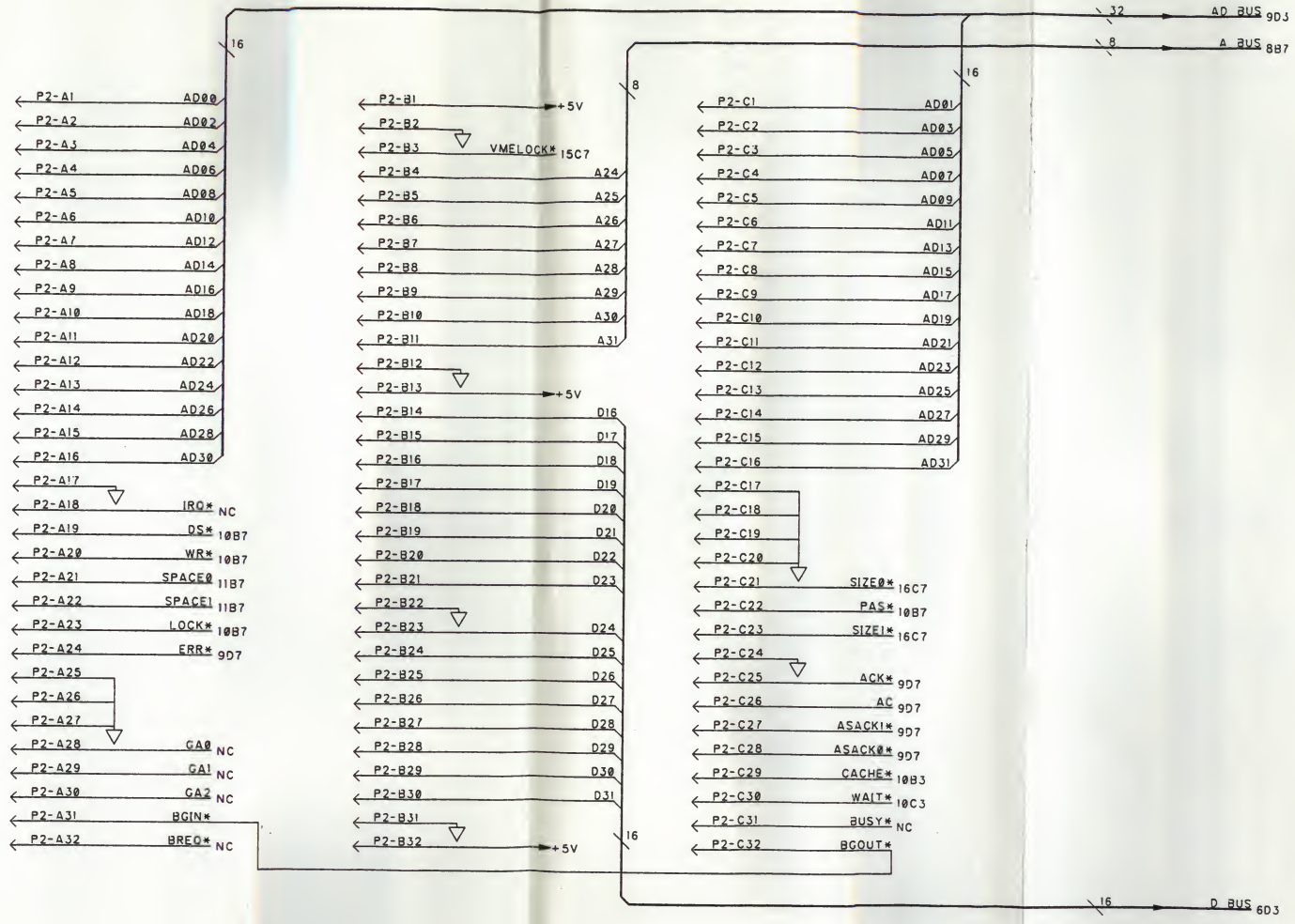
**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 2 OF 25)**




P1 CONNECTOR

63DW3500B0C REV E SH 3 OF 25

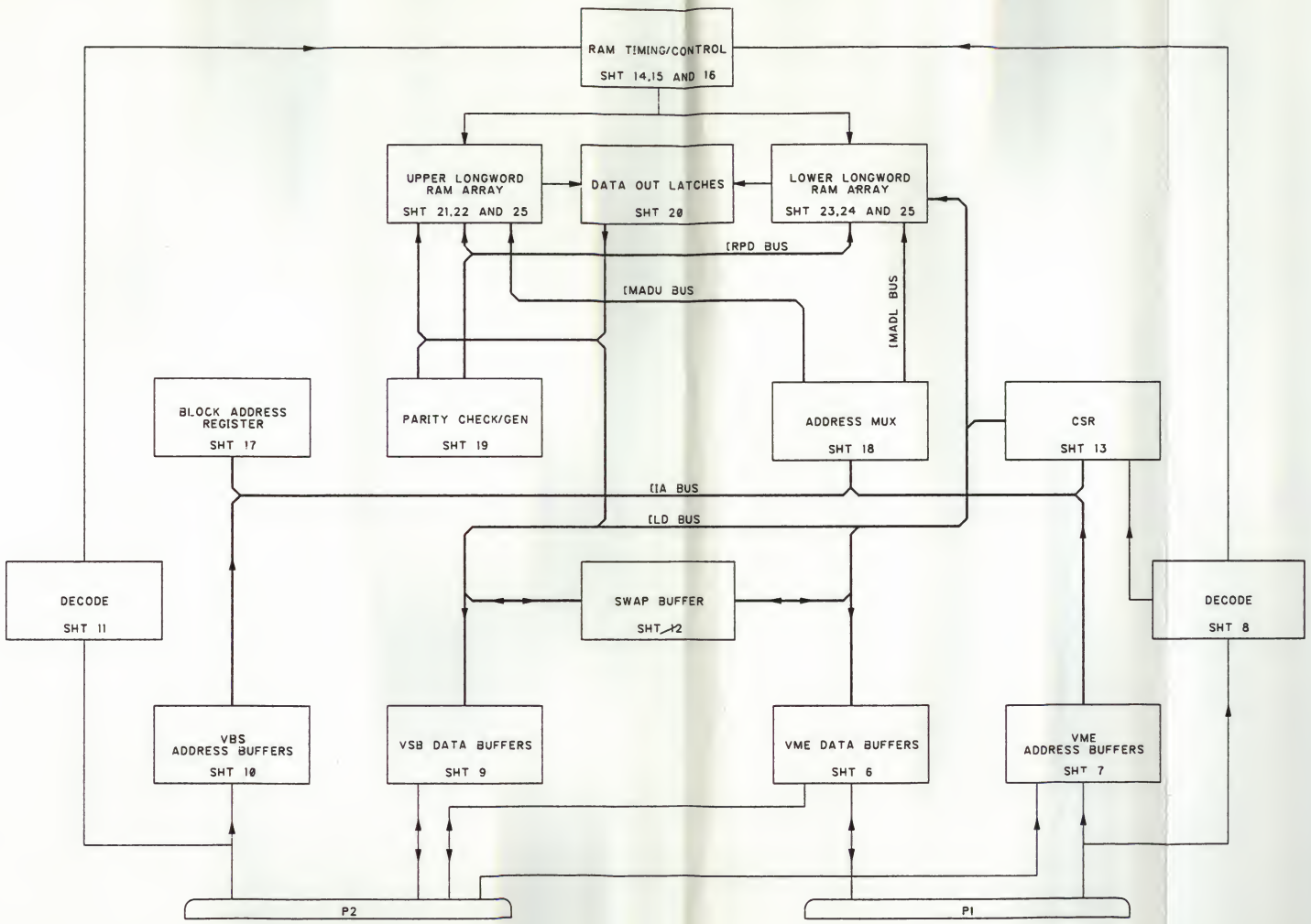
**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 3 OF 25)**




P2 CONNECTOR

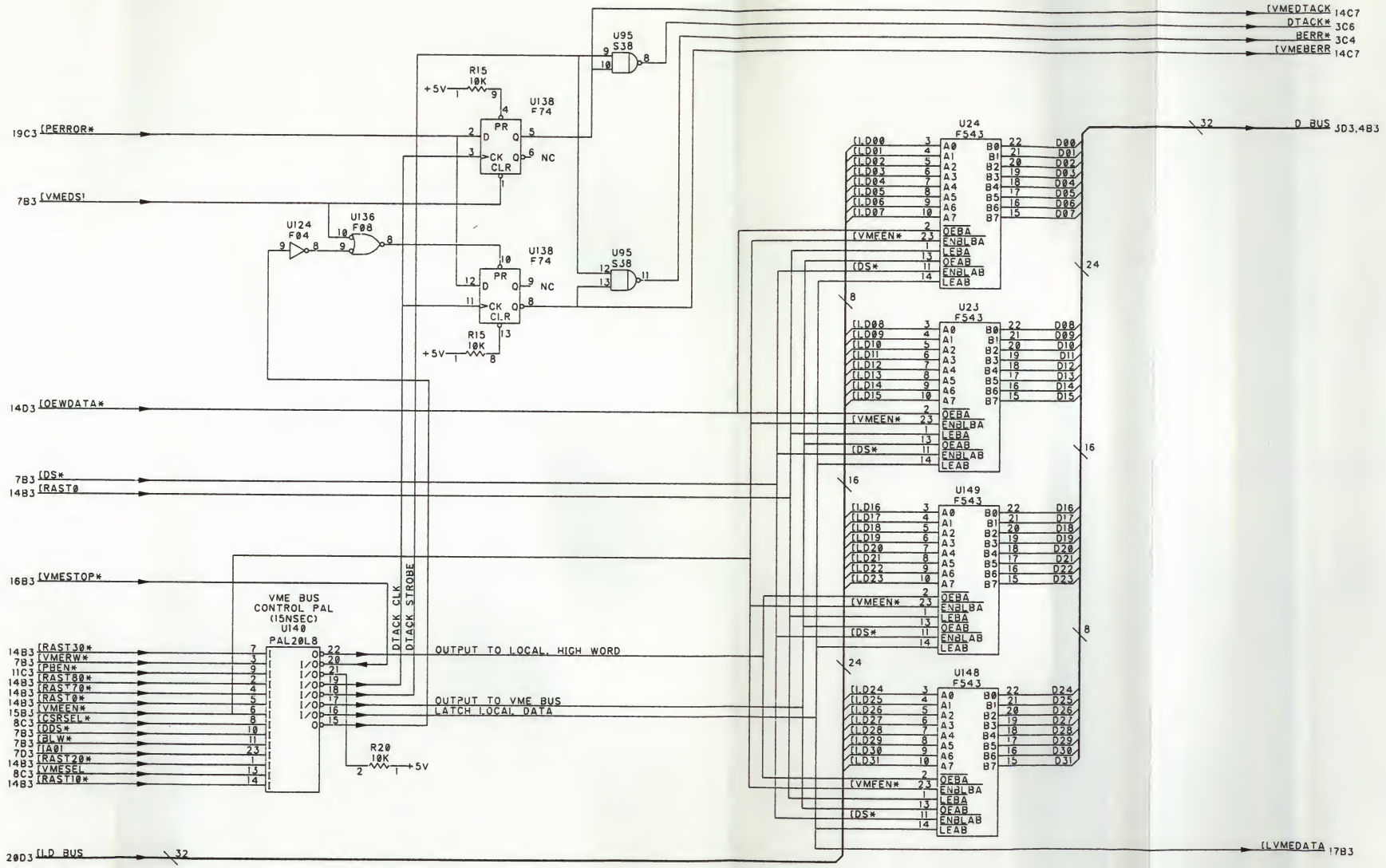
63DW3500B0C REV E SH 4 OF 25

**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 4 OF 25)**



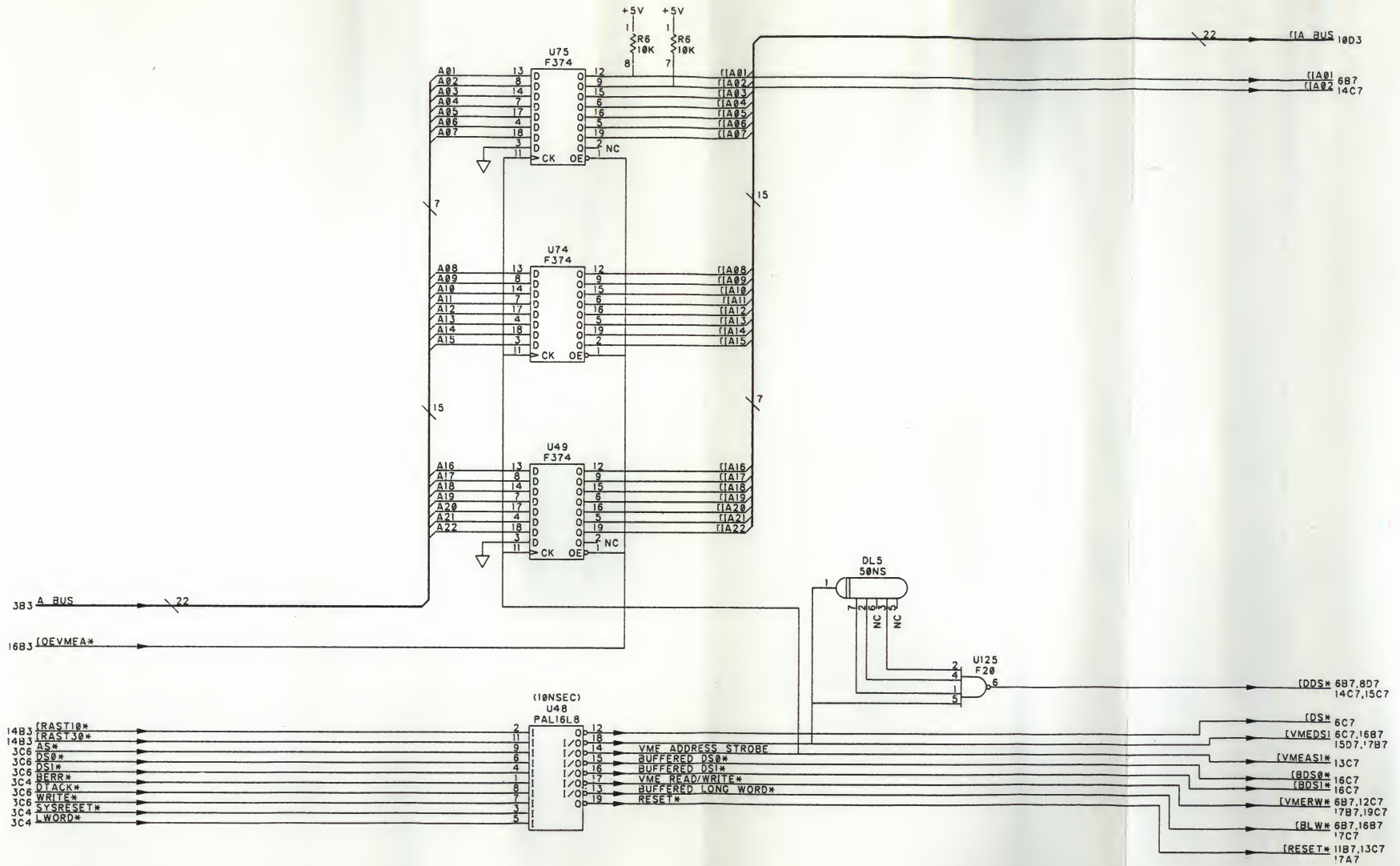

BLOCK DIAGRAM
63DW3500B0C REV E SH 5 OF 25

**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 5 OF 25)**



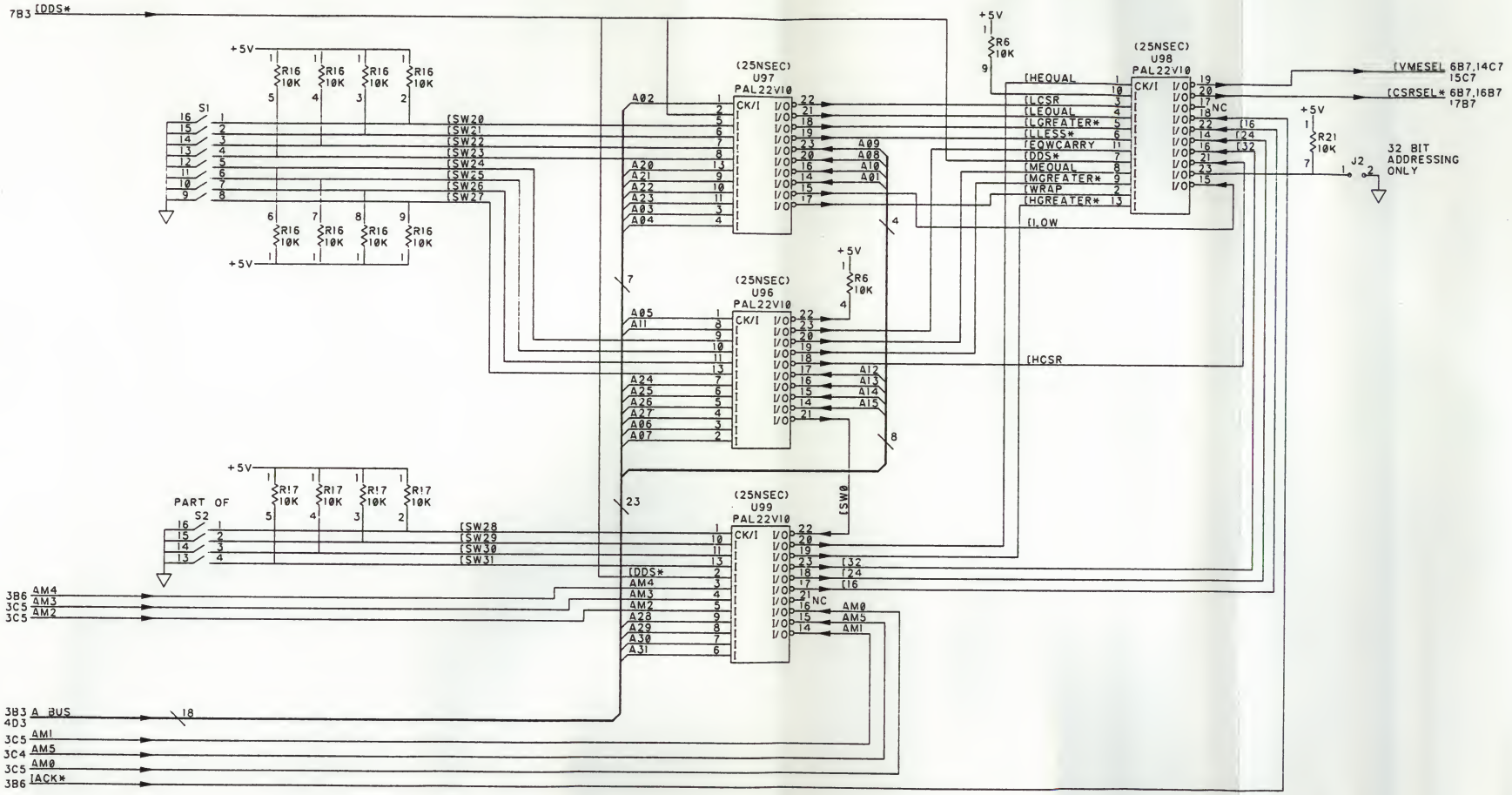

VME DATA BUS INTERFACE
63DW3500B0C REV E SH 6 OF 25

**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 6 OF 25)**




VME ADDRESS INTERFACE
63DW3500B0C REV E SH 7 OF 25

**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 7 OF 25)**




VME ADDRESS DECODE
63DW3500B0C REV E SH 8 OF 25

**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 8 OF 25)**

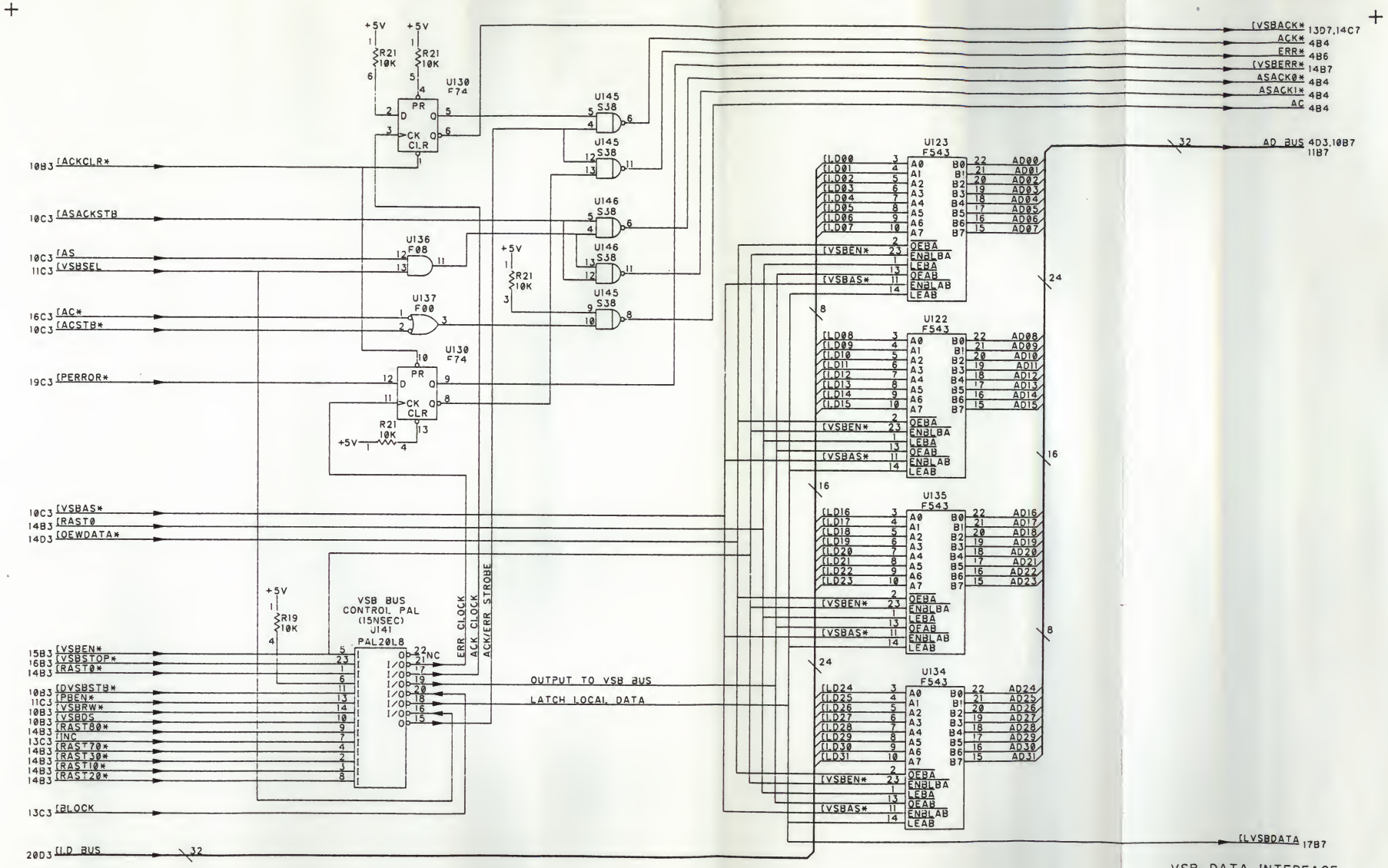
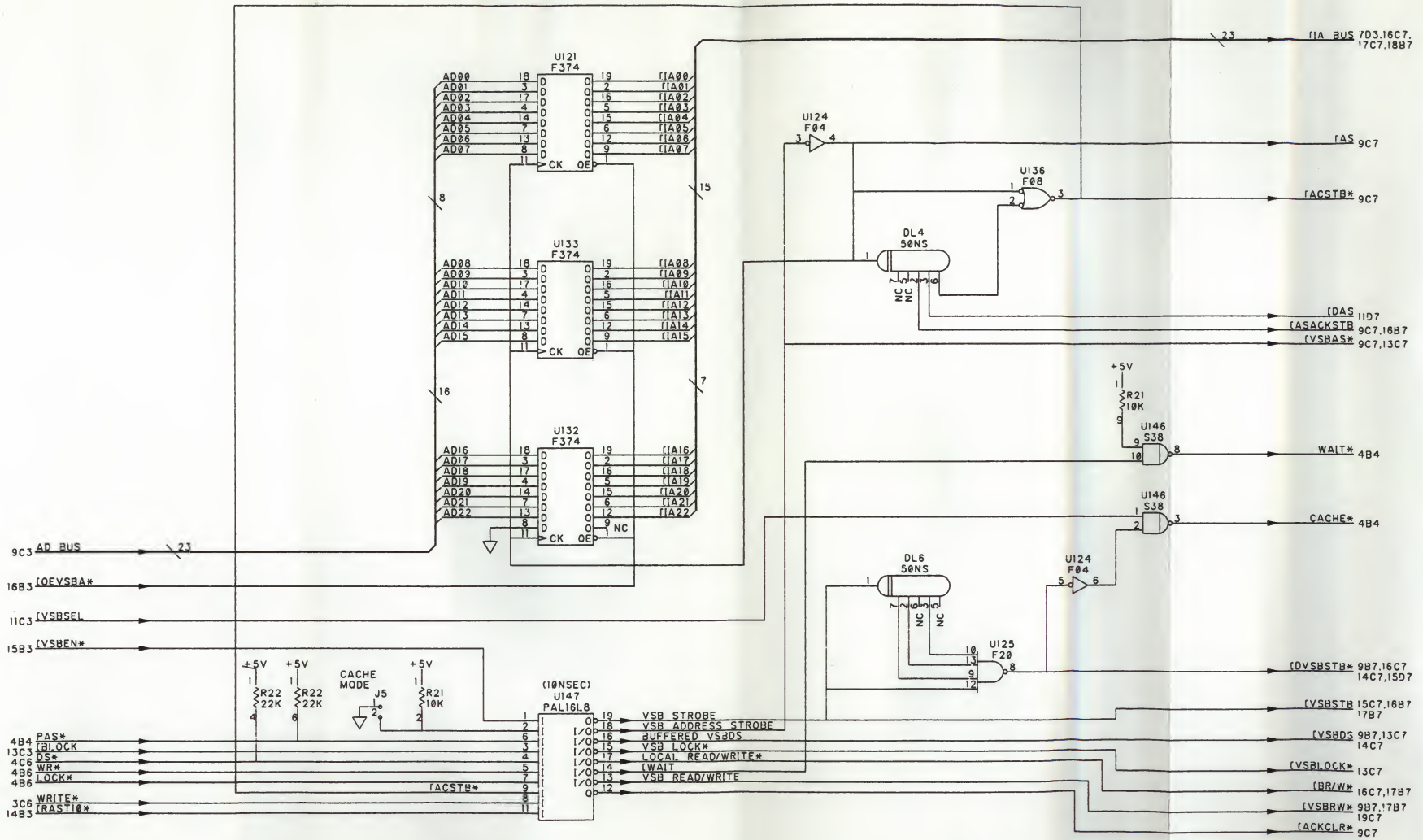
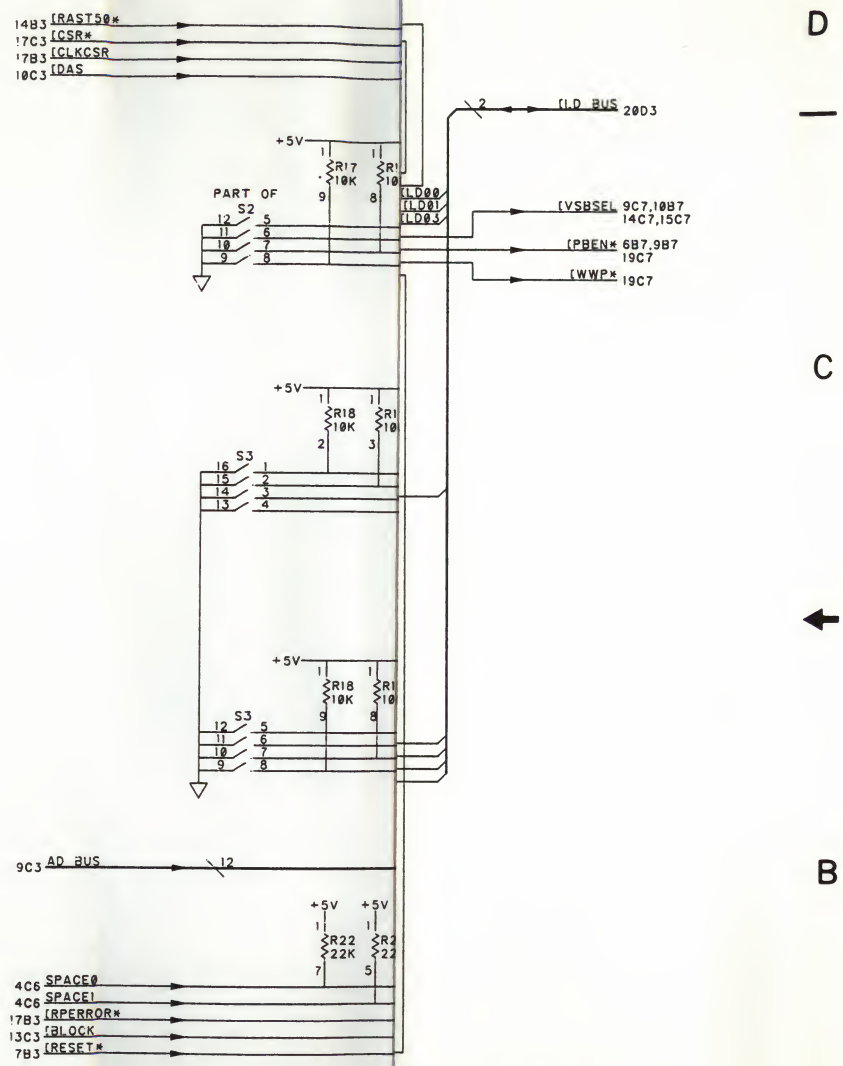



**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 9 OF 25)**




VSB ADDRESS BUFFERS
63DW3500B0C REV E SH 10 OF 25

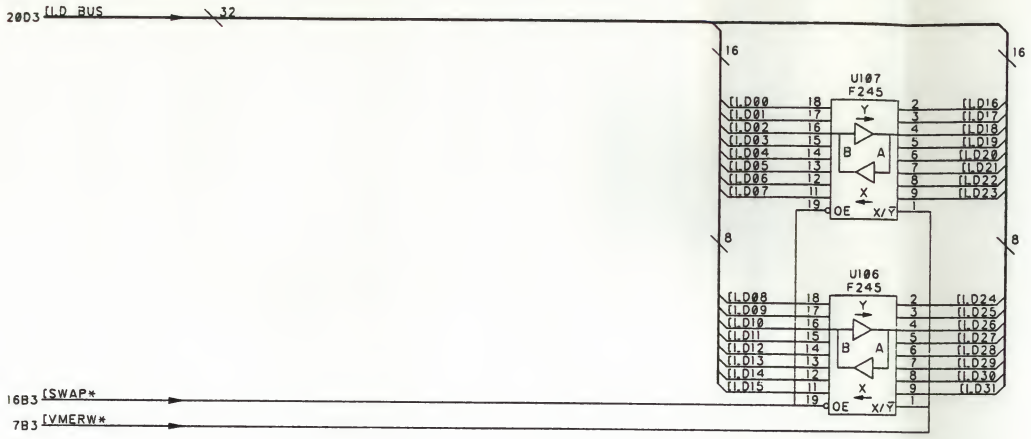
**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 10 OF 25)**




VSB ADDRESS DECODE

V3500B0C REV E SH 11 OF 25

**DIAGRAM (SHEET 11 OF 25)**

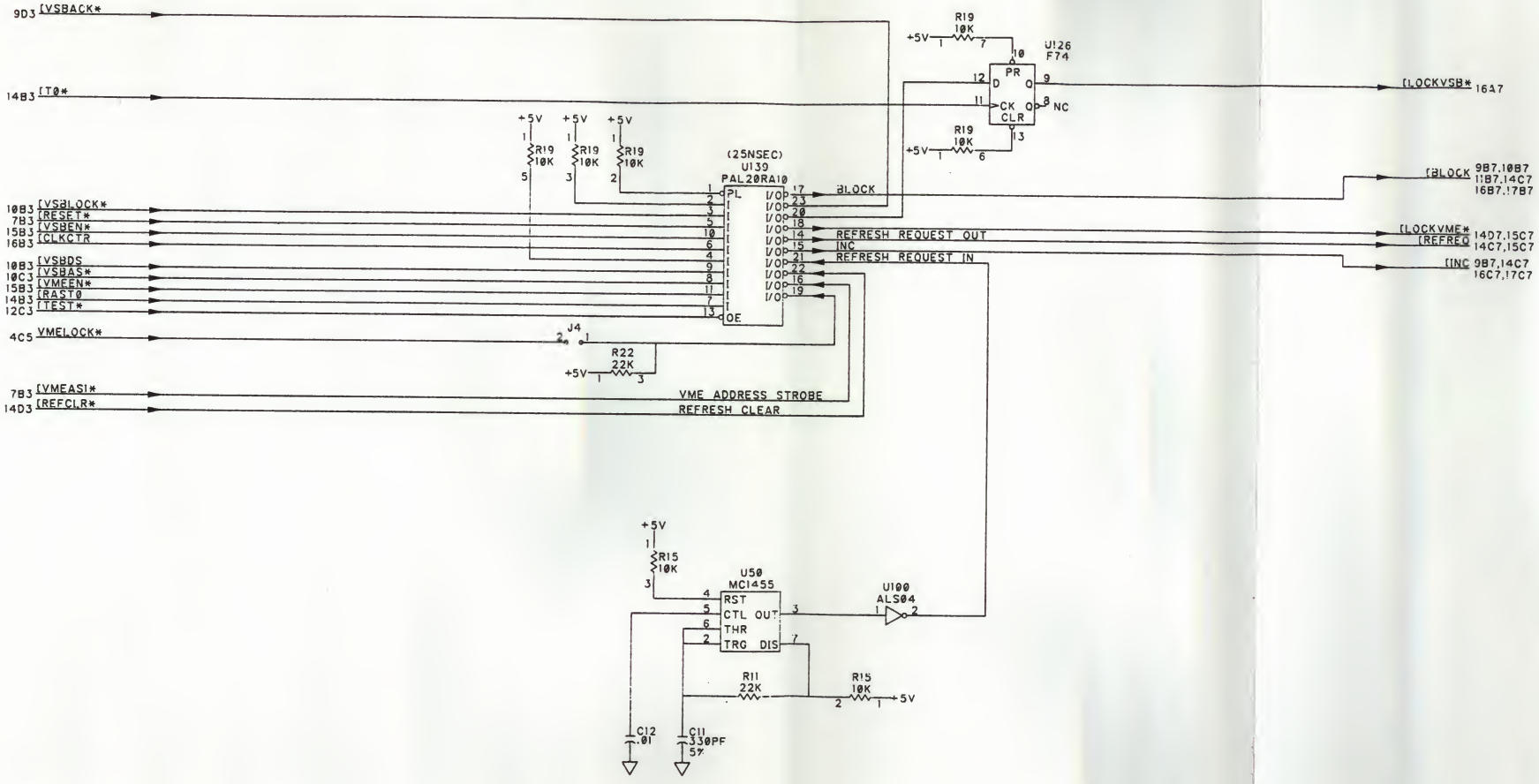




SWAP BUFFERS

63DW3500B0C REV E SH 12 OF 25

**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 12 OF 25)**




REFRESH
63DW3500B0C REV E SH 13 OF 25

**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 13 OF 25)**

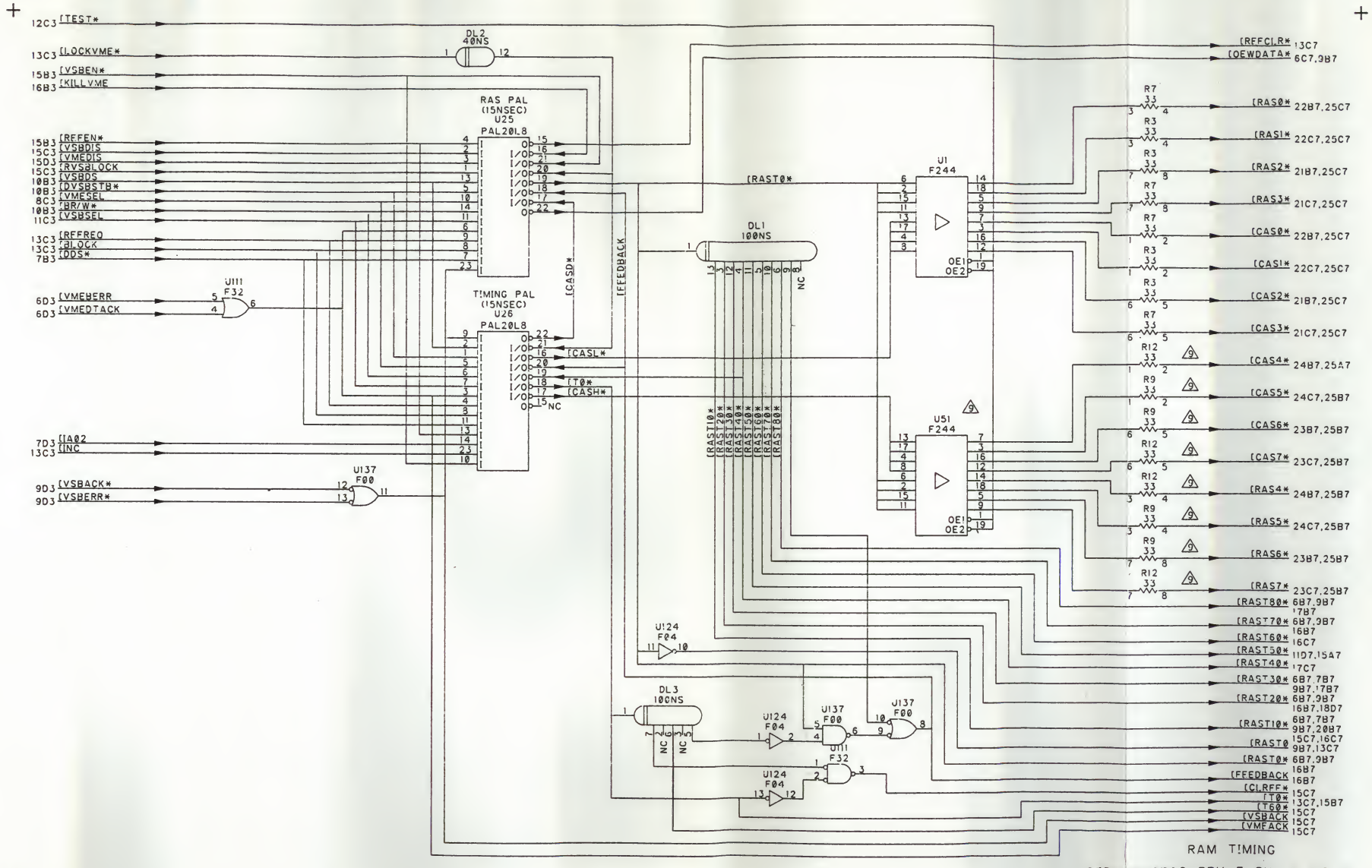
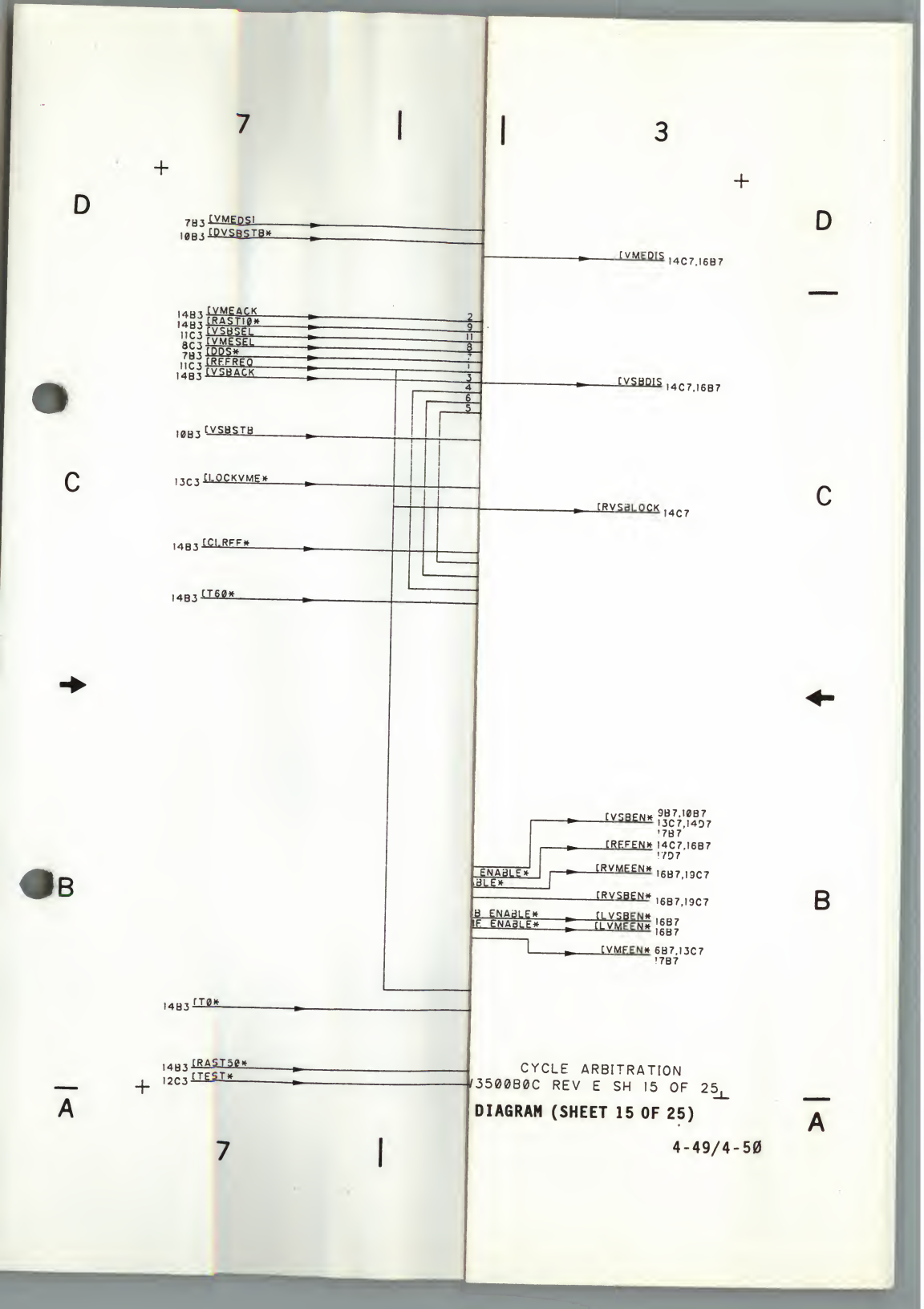
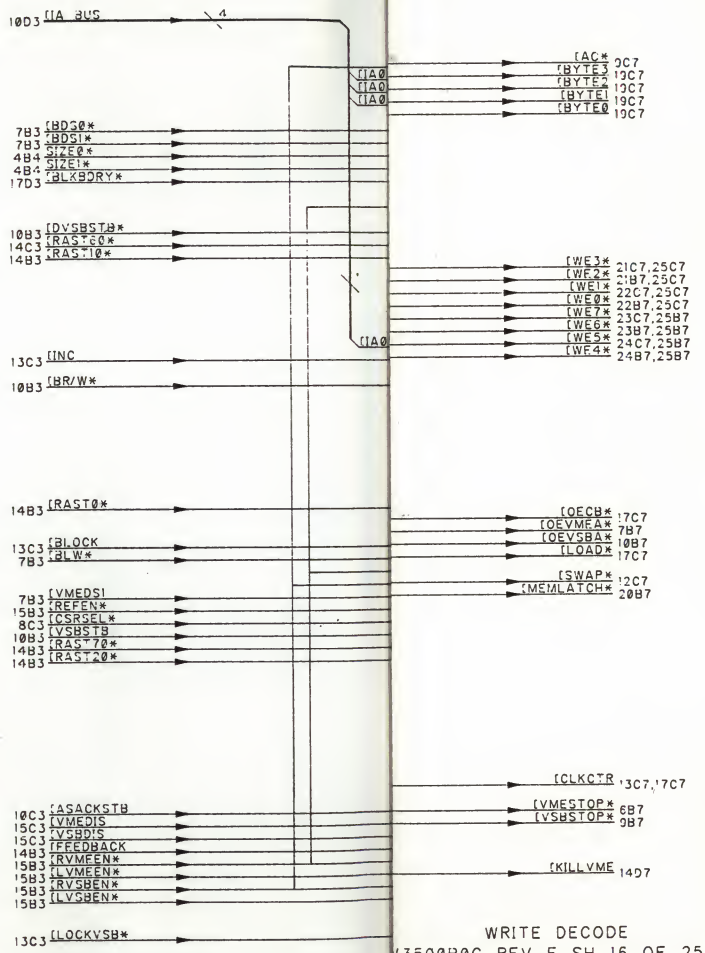



**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 14 OF 25)**




CYCLE ARBITRATION
3500B0C REV E SH 15 OF 25

**DIAGRAM (SHEET 15 OF 25)**

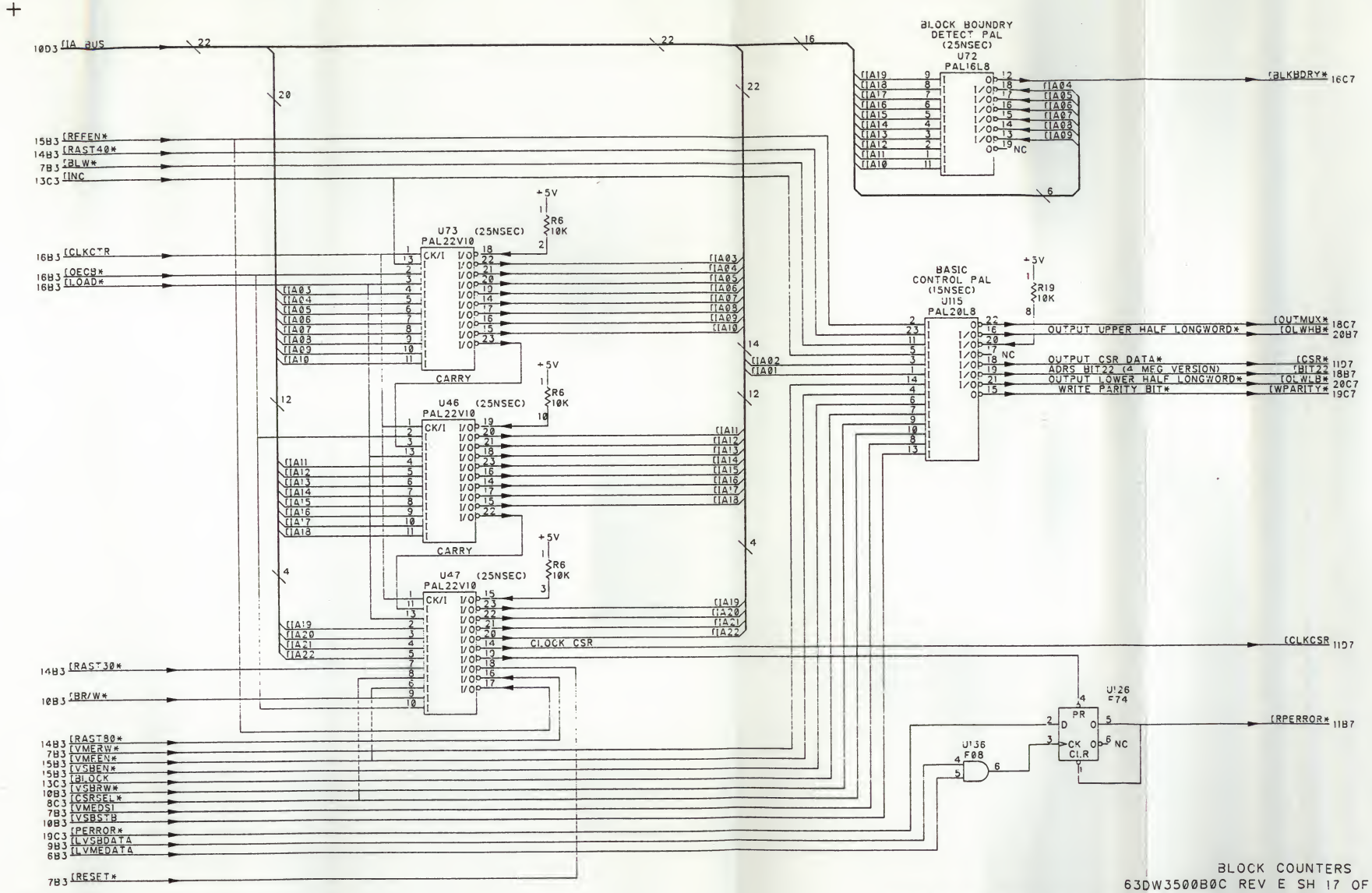



WRITE DECODE

V3500B0C REV E SH 16 OF 25

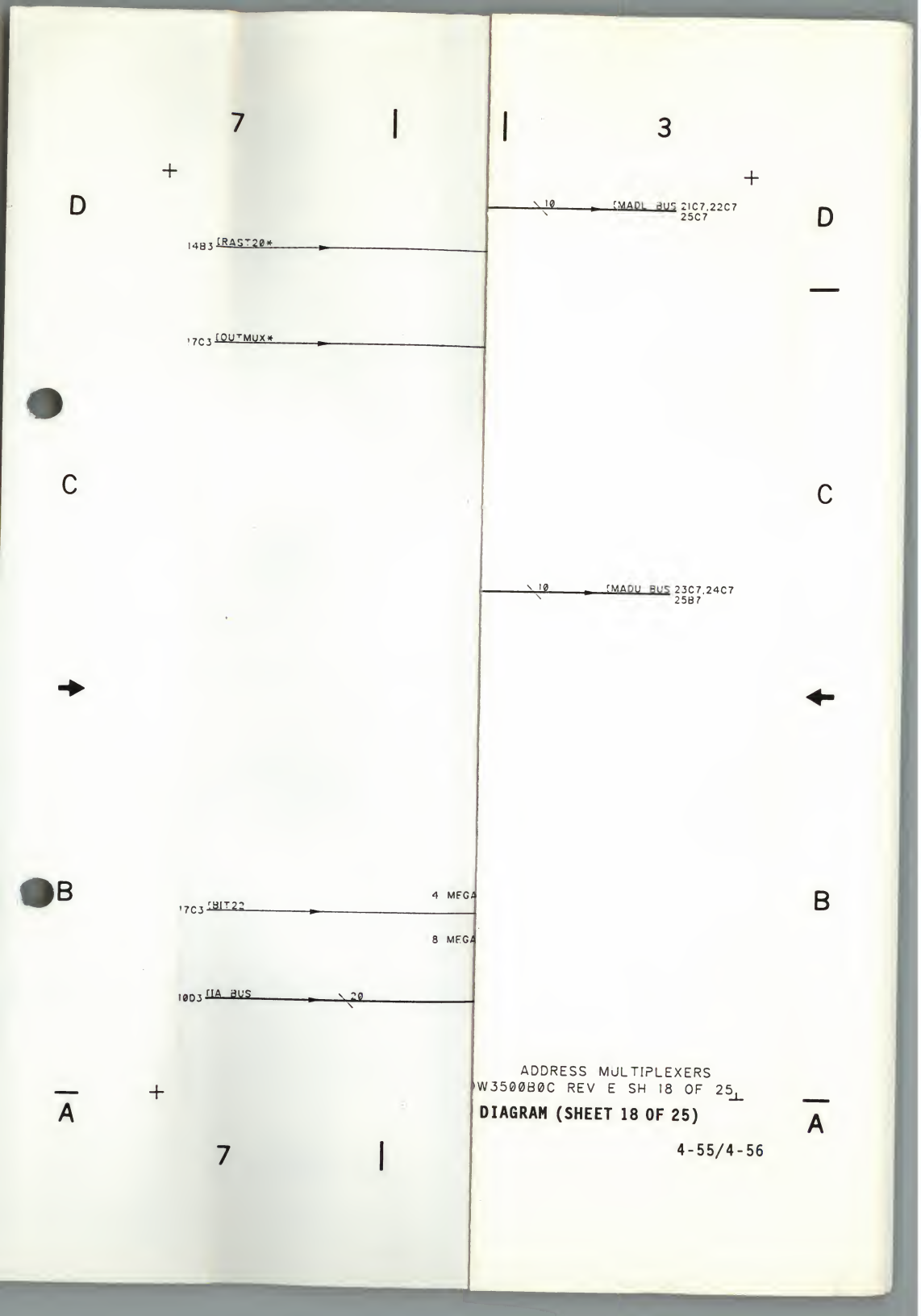
**DIAGRAM (SHEET 16 OF 25)**

4-51/4-52




BLOCK COUNTERS
63DW3500B0C REV E SH 17 OF 25

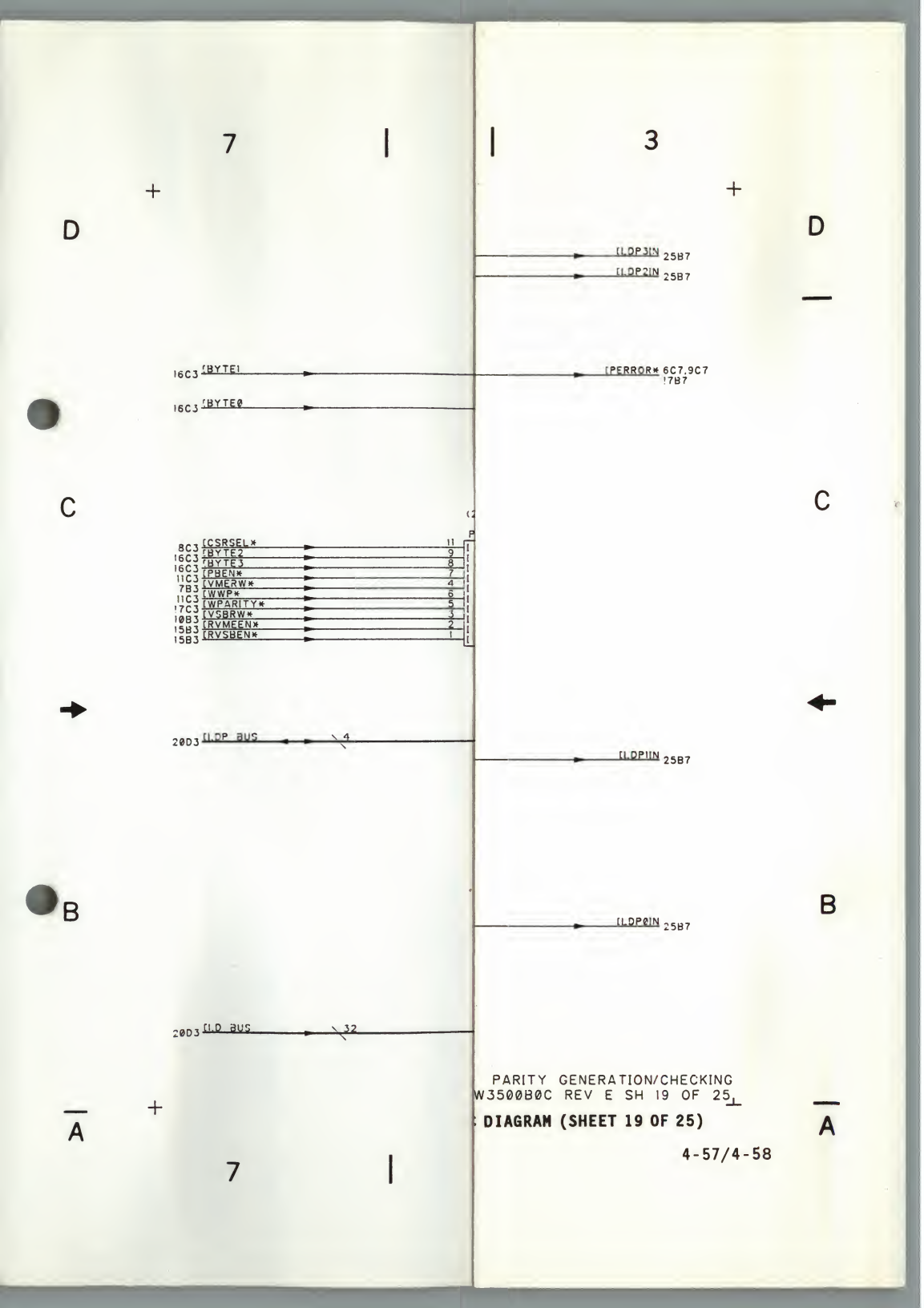
**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 17 OF 25)**




ADDRESS MULTIPLEXERS
W3500B0C REV E SH 18 OF 25

**DIAGRAM (SHEET 18 OF 25)**

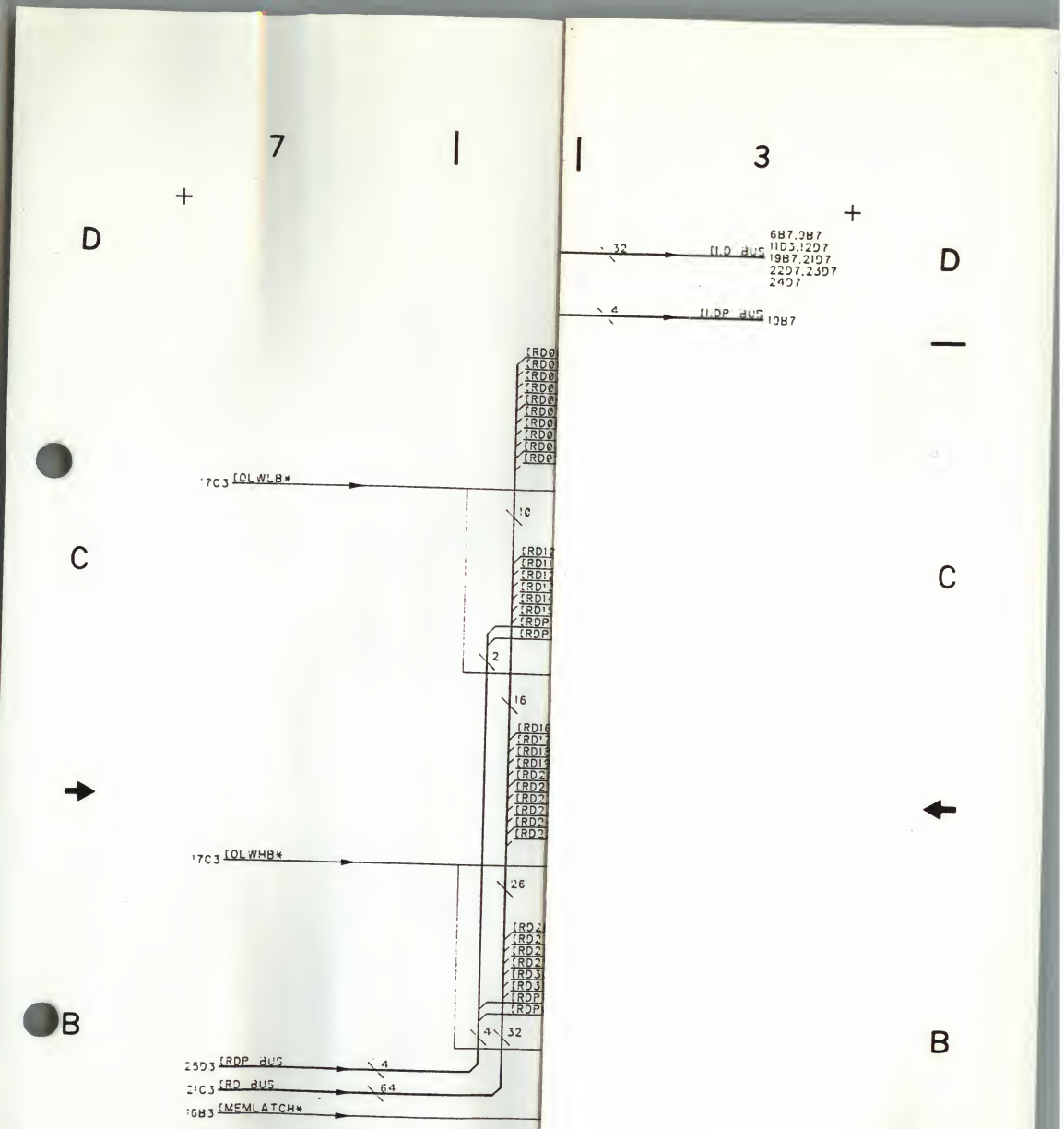
4-55/4-56




PARITY GENERATION/CHECKING
W3500B0C REV E SH 19 OF 25

**DIAGRAM (SHEET 19 OF 25)**

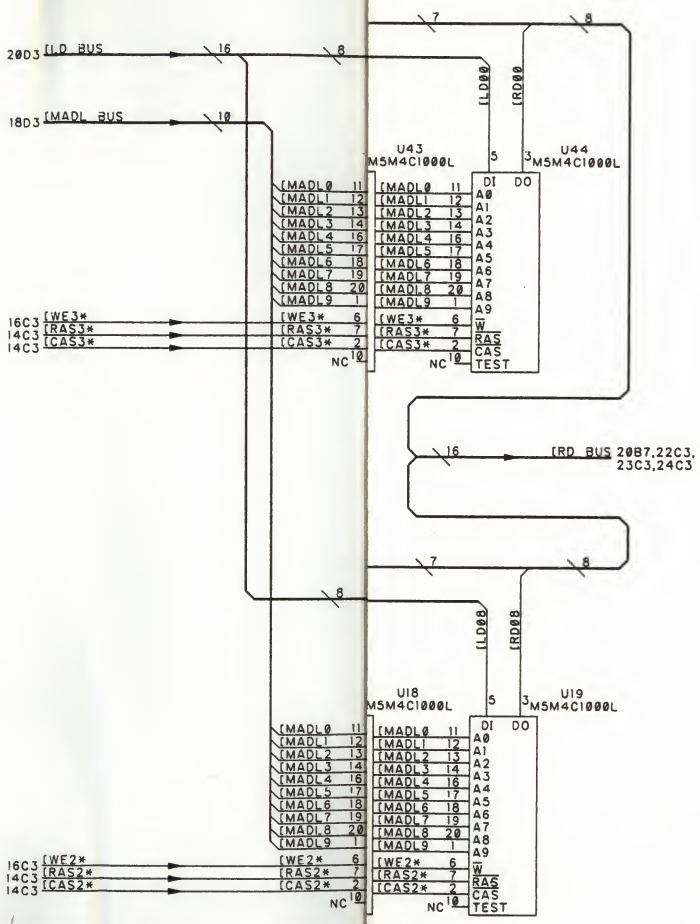
4-57/4-58




MEMORY OUT DATA LATCHES
3500B0C REV E SH 20 OF 25

**DIAGRAM (SHEET 20 OF 25)**

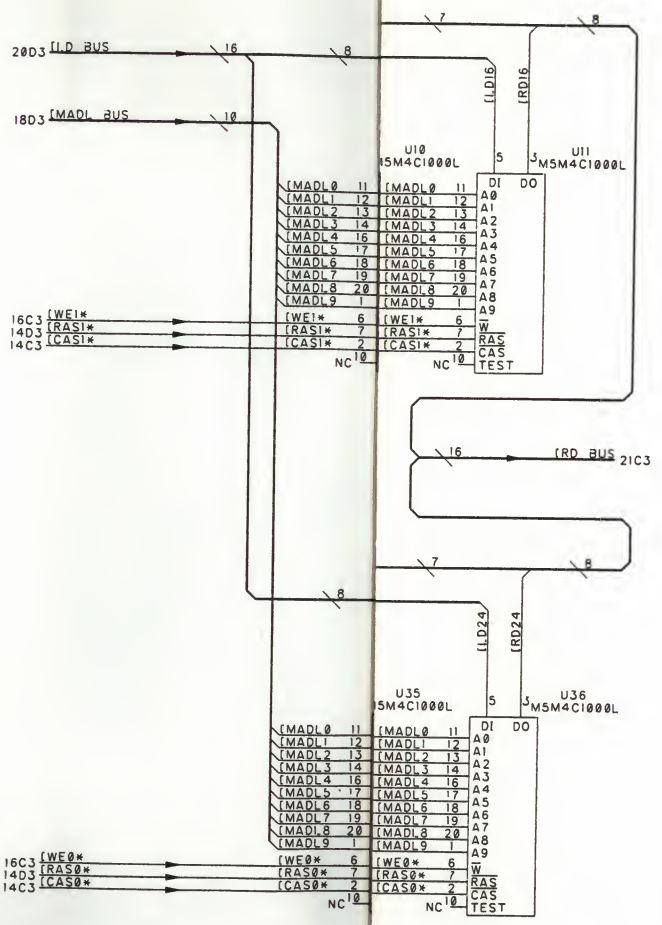
4-59/4-60




VME224 DRAM- LOWER
BYTES 2 AND 3
DW3500B0C REV E SH 21 OF 25

**IC DIAGRAM (SHEET 21 OF 25)**

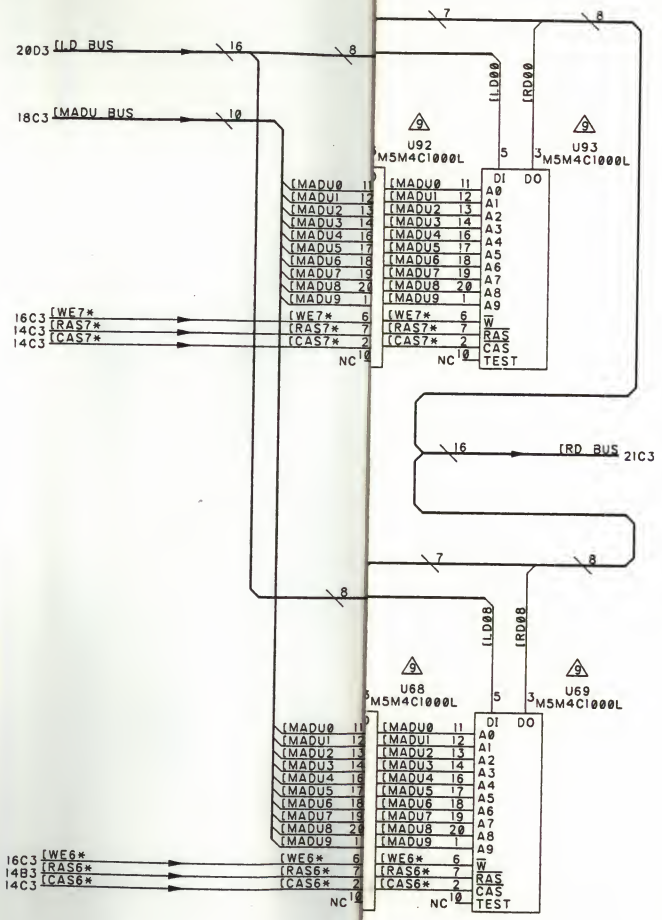
4-61/4-62




VME224 DRAM- LOWER
BYTES 0 AND 1
W3500B0C REV E SH 22 OF 25

**C DIAGRAM (SHEET 22 OF 25)**

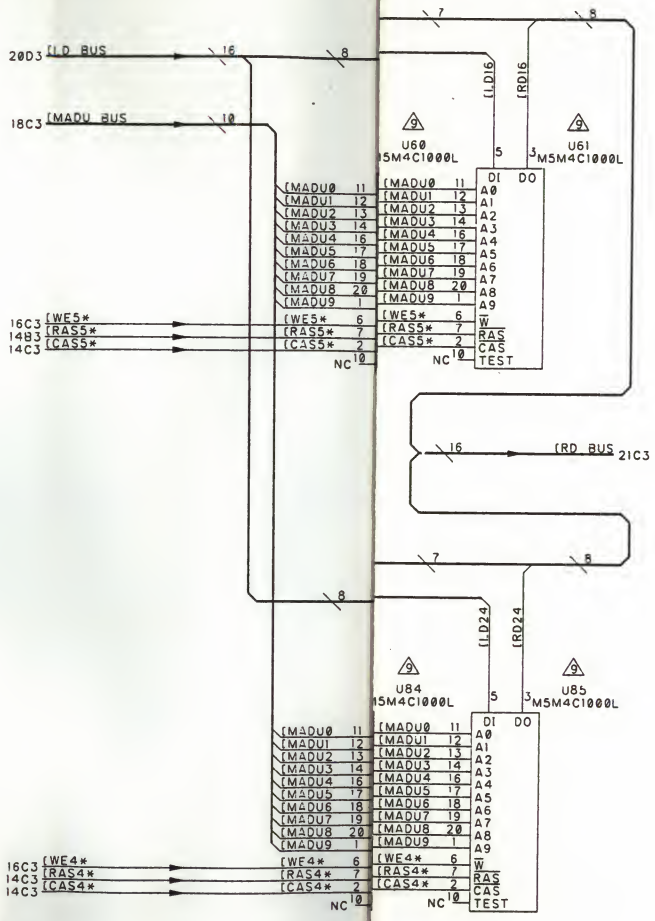
4-63/4-64




VME224 DRAM- UPPER
BYTES 2 AND 3
DW3500B0C REV E SH 23 OF 25

**IC DIAGRAM (SHEET 23 OF 25)**

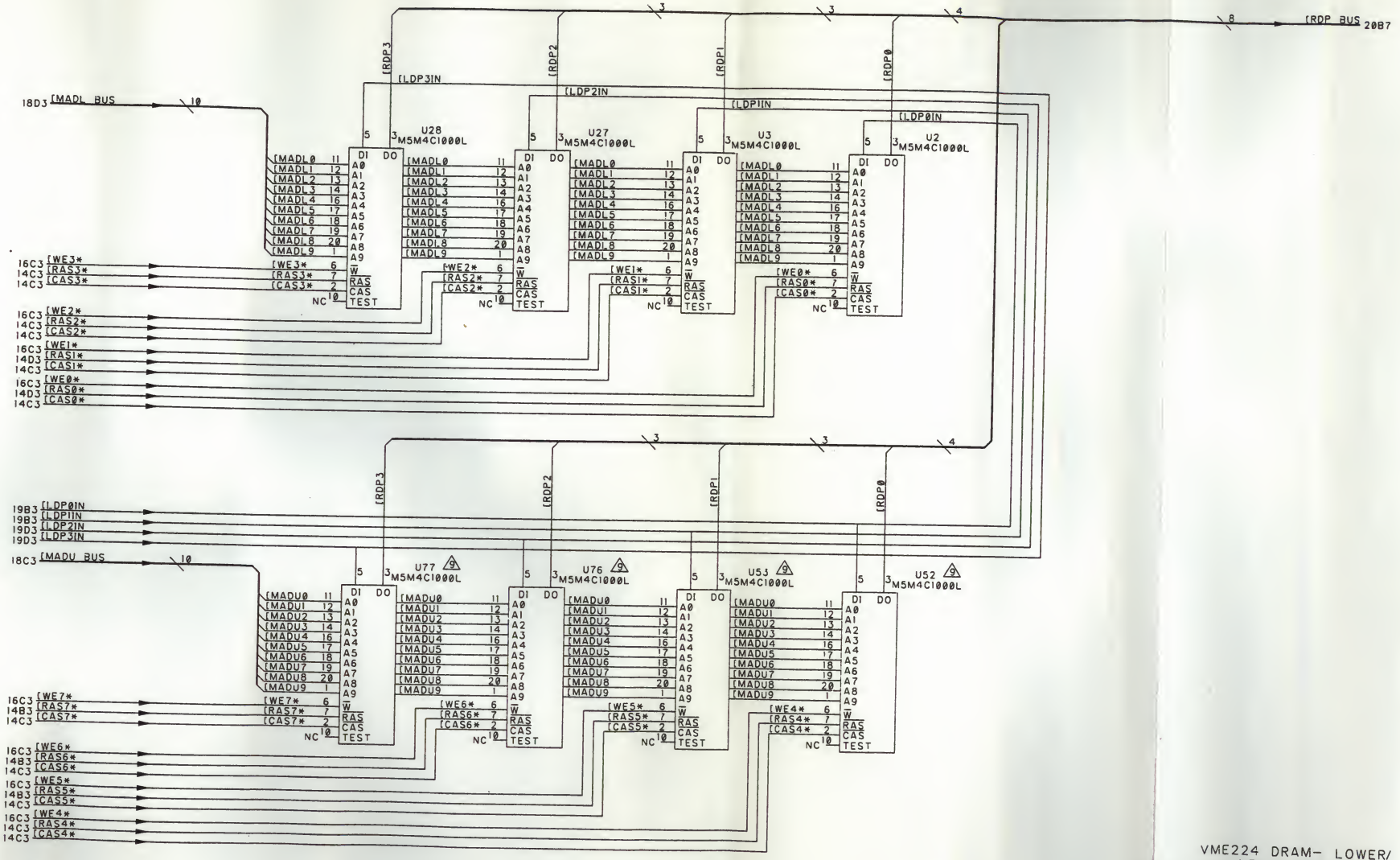
4-65/4-66




VME224 DRAM- UPPER
BYTES 0 AND 1
W3500B0C REV E SH 24 OF 25

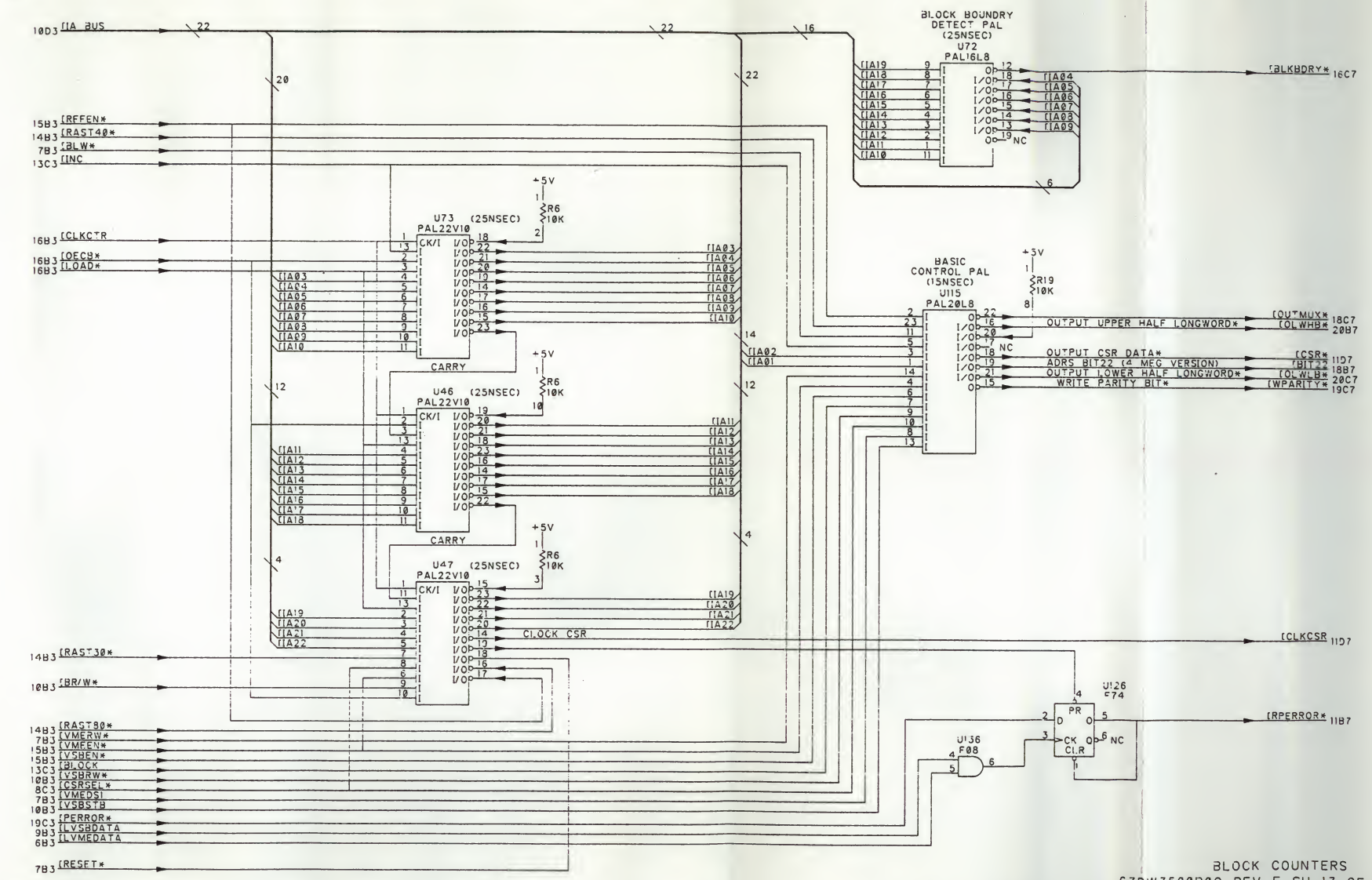
**C DIAGRAM (SHEET 24 OF 25)**

4-67/4-68




VME224 DRAM- LOWER/
UPPER PARITY
63DW3500B0C REV E SH 25 OF 25

**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 25 OF 25)**




BLOCK COUNTERS
63DW3500B0C REV E SH 17 OF 25

**FIGURE 4-2. MVME224 SCHEMATIC DIAGRAM (SHEET 17 OF 25)**

**CONVERSION LIST**

**MVME224-2 8M byte Memory Module**

| Part Number | 12 NC Number | Description |
|---|---|---|
| 76430773 | 5322 209 73869 | IC DELAY LINE 40NS |
| 01NW9804C33 | 5322 209 72706 | IC DELAY LINE 40NS |
| 01NW9804C80 | 5322 209 73905 | IC DELAY LINE 100NS |
| 06SW-962A29 | | RES 150E 5% 0.125W |
| 06SW-962A81 | | RES 22K . 5% 0.125W |
| 21NW9604A58 | | CAP 330PFF 50V 5% |
| 21NW9632A03 | 5322 122 33424 | CAP 0.1UF 50VDC |
| 21SW992C014 | | CAP 0.010F 50V CER |
| 23NW9618A82 | 5322 124 41431 | CAP 22UF 25V ELE |
| 40NW9801A34 | 5322 277 11068 | SWITCH DIP 8 POS. |
| 48NW9612A59 | 5322 130 80846 | LED GREEN |
| 51-W4804C89 | | IC PAL |
| 51-W4804C91 | | IC PAL |
| 51-W4939B18 | | IC PAL |
| 51-W5120C18 | | IC PAL |
| 51-W5120C19 | | IC PAL |
| 51-W5120C27 | | IC PROM |
| 51-W5120C30 | | IC PAL |
| 51-W5388B12 | | IC PAL |
| 51-W5388B13 | | IC PAL |
| 51-W5388B14 | | IC PAL |
| 51-W5388B15 | | IC PAL |
| 51-W5388B16 | | IC PAL |
| 51-W5388B17 | | IC PAL |
| 51-W5388B18 | | IC PAL |
| 51-W5388B20 | | IC PAL |
| 51-W5388B21 | | IC PAL |
| 51-W5388B22 | | IC PAL |
| 51-W5388B23 | | IC PAL |
| 51-W5388B34 | | IC PAL |
| 51-W5388B36 | | IC PAL |
| 51-W5388B37 | | IC PAL |
| 51-W5388B38 | | IC PAL |
| 51-W5388B39 | | IC PAL |
| 51-W5388B40 | | IC PAL |
| 51-W5388B42 | | IC PAL |
| 51-W5388B54 | | IC PAL |
| 51-W5388B55 | | IC PAL |
| 51-W5388B60 | | IC PAL |
| 51-W5449B52 | | IC PAL |
| 51-W5449B64 | | IC PAL |

| Part Number | 12 NC Number | Description |
|---|---|---|
| 51-W5473B08 | | IC PAL |
| 51AW4591D23 | | IOC PAL |
| 51AW4591D24 | | IOC PAL |
| 51AW5100B09 | | IC PAL |
| 51AW5120B72 | | IC PAL |
| 51AW5120B73 | | IC PAL |
| 51AW5120B75 | | IC PAL |
| 51AW5120B76 | | IC PAL |
| 51NW9615B65 | 5322 209 72472 | IC MC1455P1 |
| 51NW9615C24 | 5322 209 81634 | IC SN74LS32N |
| 51NW9615F85 | 5322 209 85677 | IC SN74S38N |
| 51NW9615J39 | 5322 209 81474 | IC 74F74PC |
| 51NW9615K18 | 5322 209 81533 | IC 74F373PC |
| 51NW9615K47 | 5322 209 81128 | IC 74F244PC |
| 51NW9615K60 | | IC 74F158APC |
| 51NW9615K65 | 5322 209 81538 | IC 74F64PC |
| 51NW9615K66 | 5322 209 71609 | IC 74F32PC |
| 51NW9615K67 | 5322 209 82013 | IC 74F20PC |
| 51NW9615K70 | 5322 209 72035 | IC SN74AS08N/74F08PC |
| 51NW9615K71 | 5322 209 81577 | IC 74F04PC |
| 51NW9615K73 | 5322 209 81534 | IC 74F00PC |
| 51NW9615K99 | 5322 209 81909 | IC 74F374PC |
| 51NW9615M90 | 5322 209 82169 | IC 74F245PC |
| 51NW9615R16 | 5322 209 71475 | IC SN74ALS04AN |
| 51NW9615R36 | 5322 209 73086 | IC 74F543PC |
| 51NW9615U44 | | IC M5M4C1000L-10 |
| 51NW9615V22 | | IC TC511001Z-10 |
| 51NW9615V91 | | IC SN74AS280N |
| 51NW9615W26 | | IC DS1000M-100 |
| 51NW9615W31 | | IC SN74AS841NT |
| 51NW9615W46 | | IC DS1000M-50 |
| 51NW9626A49 | 5322 116 90516 | RNW 7X10K |
| 51NW9626B01 | | RNW 4-330 8P |
| 51NW9626B47 | | RNW 9-22K 10P |
| 51NW9626B56 | 5322 116 90502 | RNW 9X10K |
| 64-W5501B01 | | FRONT PNL MVME224-2 |
| 84-W8500B01 | | MVME224-2 8MB PCB |